

SF2

Rev: 2.2

Page Index =====

Revision History :

1. Ver A: Initial
2. Ver B:
 - (1) Add North Bridge Fan Sink Header
 - (2) Delete SATA Crystal
 - (3) Modify USB, AUDIO, S/P DIF Out, Front Panel Headers for ACER
 - (4) Add SATA Status LED Signal via Front Panel
 - (5) Modify USB Power Source on South Bridge due to SiS AP note
 - (6) Add One More Fuse for 1394 Header
 - (7) Add SPDIFO2 Header (Pitch 2.0mm) for HP S/P DIF Out
 - (8) Modify Hardware Reset Circuit
 - (9) Modify VCCVID Power Good Circuit
 - (10) Remove IR, SIRQ Headers
 - (11) Add JP4, JP5 Headers for HP
 - (12) Modify CPU Fan Control Circuit
 - (13) Change RT9173 for DDR Vtt
 - (14) Change LAN Connector Type
3. Ver 1.0:
 - (1) Add C289, MC40 for EMI Solution
4. Ver 2.0:
 - (1) Modify USB3, USB4 Location on PCB
 - (2) Change PWM
5. Ver 2.1:
 - (1) Add IrDA, Wake on LAN, Wake on MODEM Headers for China OEM
6. Ver 2.2:
 - (1) To follow SiS AP note, modify CPUPWRGD circuit to support Intel Prescott C-stepping CPU on Page7
 - (2) Support ALC658 CODEC

1. Cover Sheet
2. Block Diagram
3. Clock & Power Distribution
4. Socket478-1
5. Socket478-2
6. Decoupling Circuit
7. SiS661FX-1 (HOST / AGP)
8. SiS661FX-2 (Memory)
9. SiS661FX-3 (VGA / HyperZip)
10. SiS661FX-4 (Power)
11. SiS964-1 (PCI / IDE / HyperZip)
12. SiS964-2 (Misc. Signals)
13. SiS964-3 (USB)
14. SiS964-4 (Power)
15. Main Clock
16. Clock Buffer
17. DDR DIMM 1, 2
18. DDR Termination
19. AGP slot
20. VGA / IDE Connectors
21. USB Connector
22. PCI Slot1, 2
23. PCI Slot3
24. LAN
25. IEEE1394
26. Audio Codec
27. Audio Interface
28. Super I/O
29. KB/MS/ROM/FDC/IR
30. COM 1,2 / LPT
31. HM/FAN/RING/LPC
32. Voltage Regulator
33. DUAL 5V, 3V& SB Regulator
34. VRD10 (CPU Vcore)
35. ATX / Panel / RTC
36. BOM and GPIO Attention



SIGNATURE


DATE

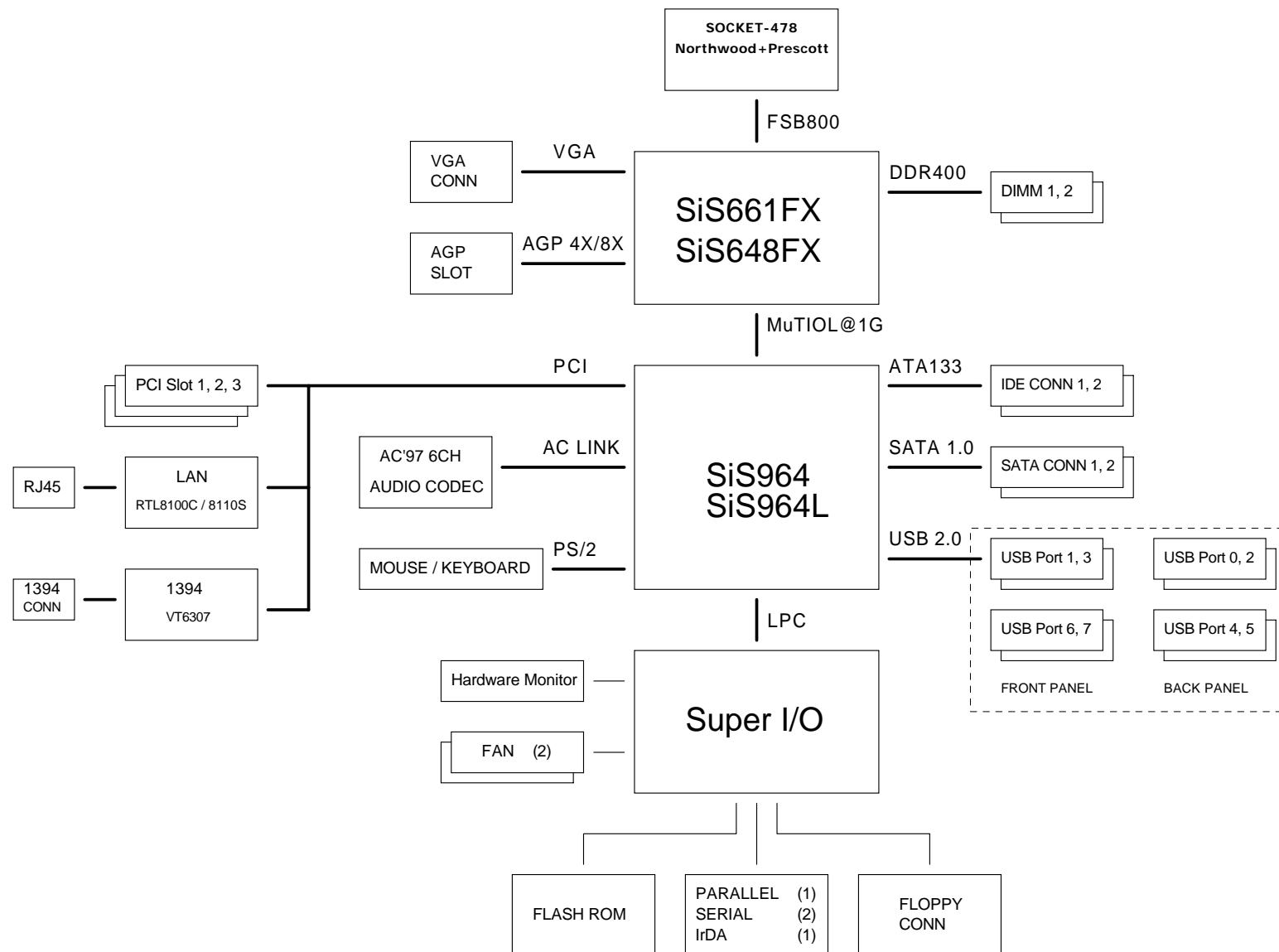
DESIGNER

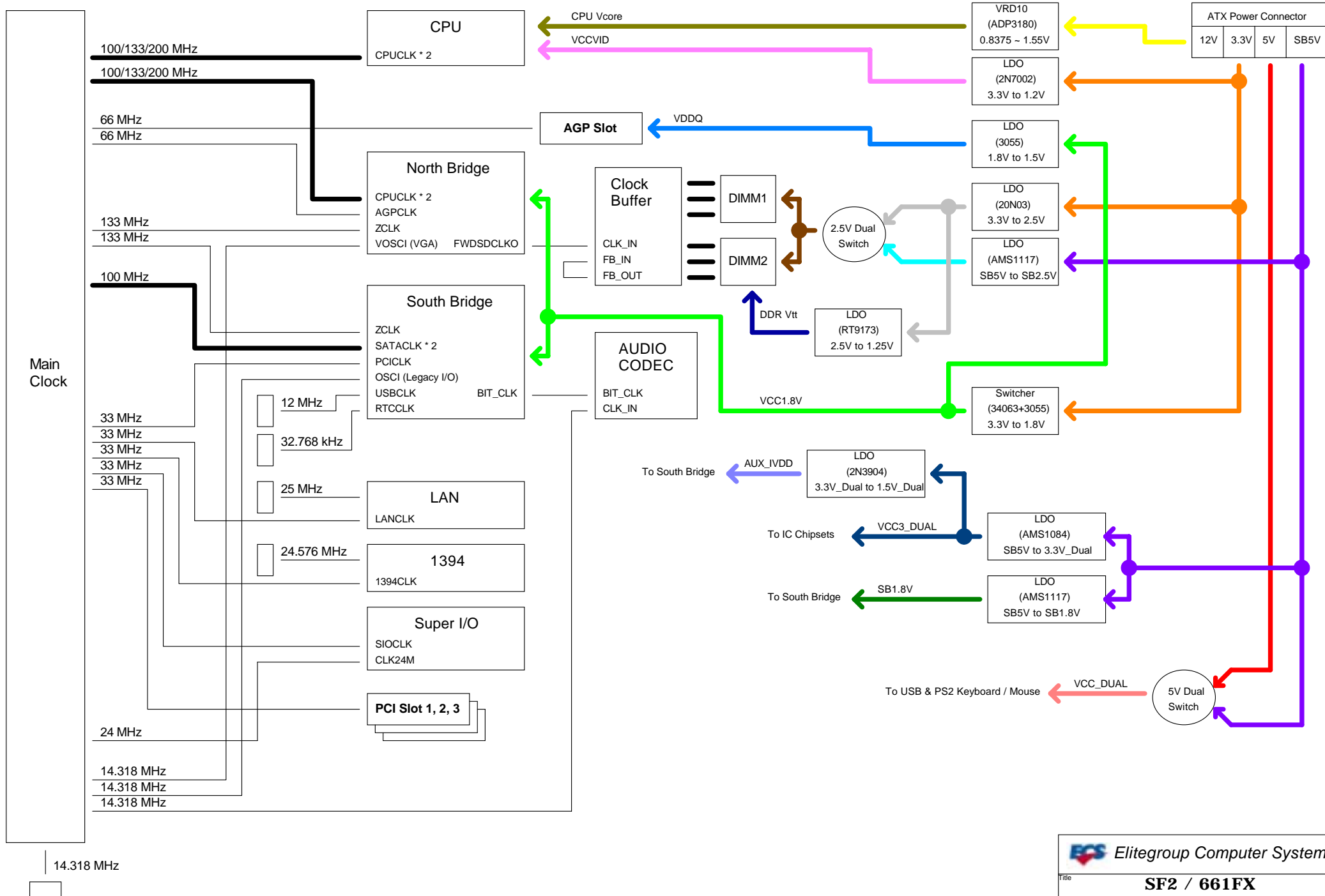
LAYOUT

CHECK

APPROVAL

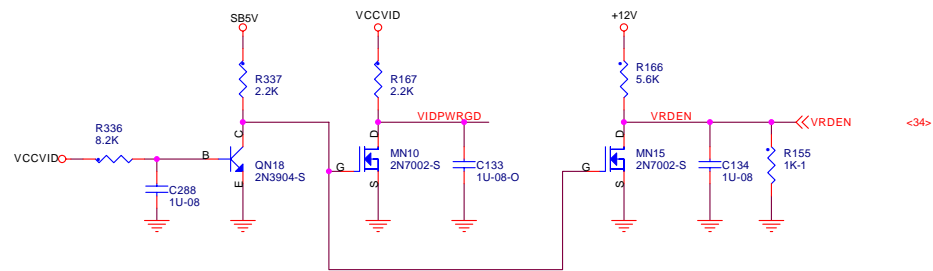
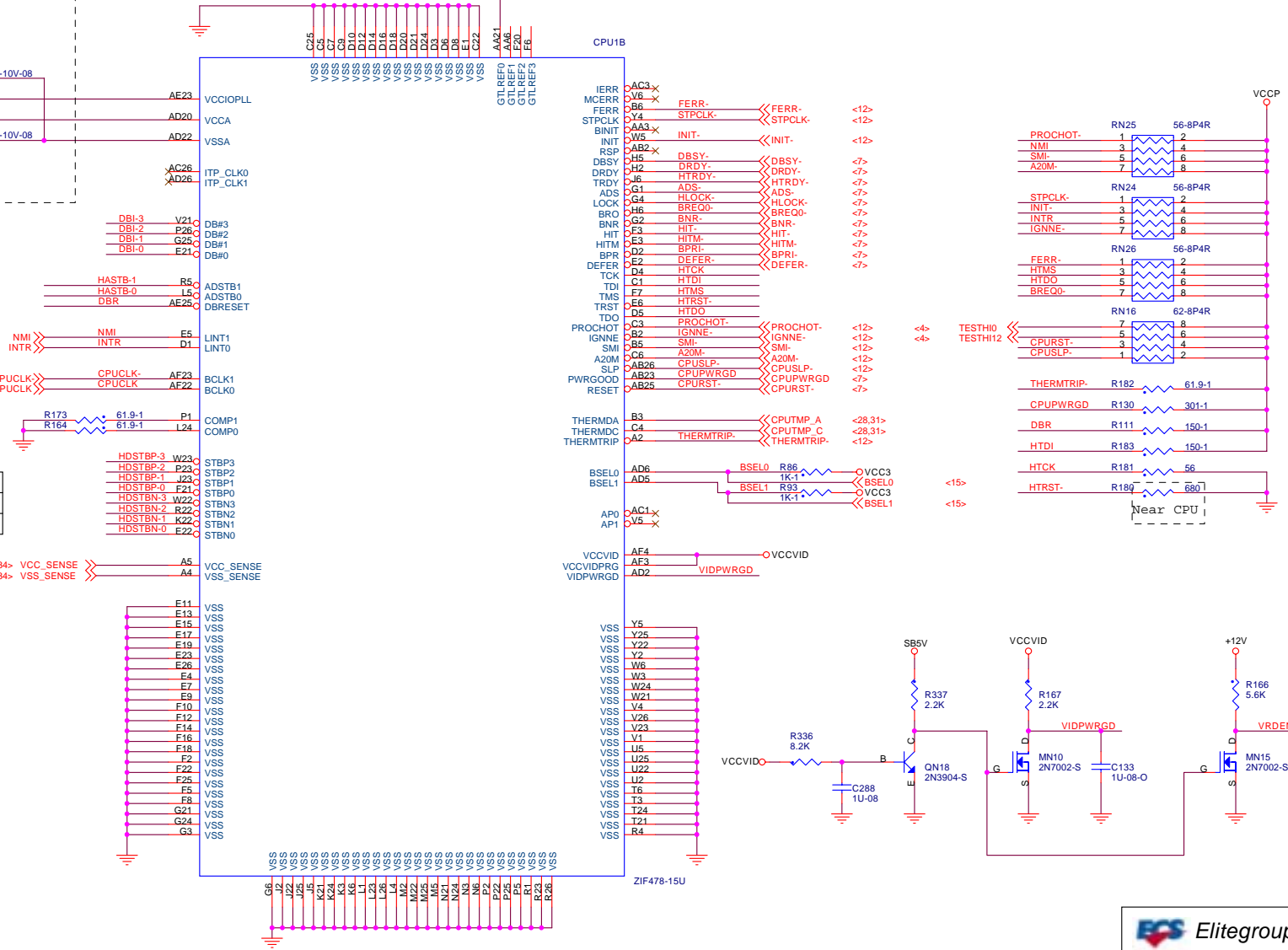
 Elitegroup Computer Systems		
Title SF2 / 661FX		
Size	Document Number	Rev
Custom	Cover Sheet	2.2
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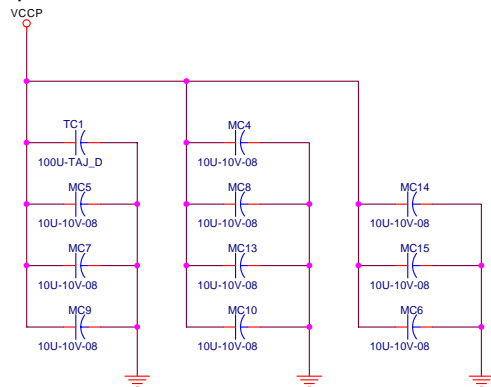


HD-[0..63] <<HD-[0..63] <7>
HA-[3..31] <<HA-[3..31] <7>
VID[0..5] <<VID[0..5] <34>
HREQ-[0..4] <<HREQ-[0..4] <7>
RS-[0..2] <<RS-[0..2] <7>

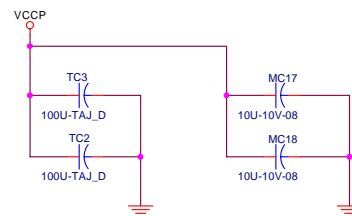




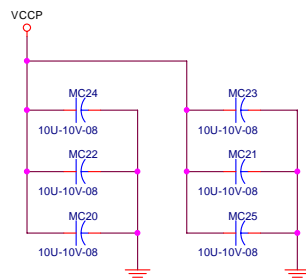
Put these capacitors at processor NORTH SIDE



Put these capacitors INSIDE PROCESSOR CAVITY

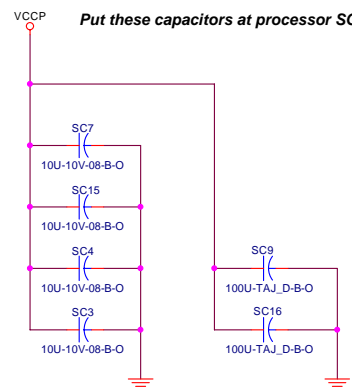


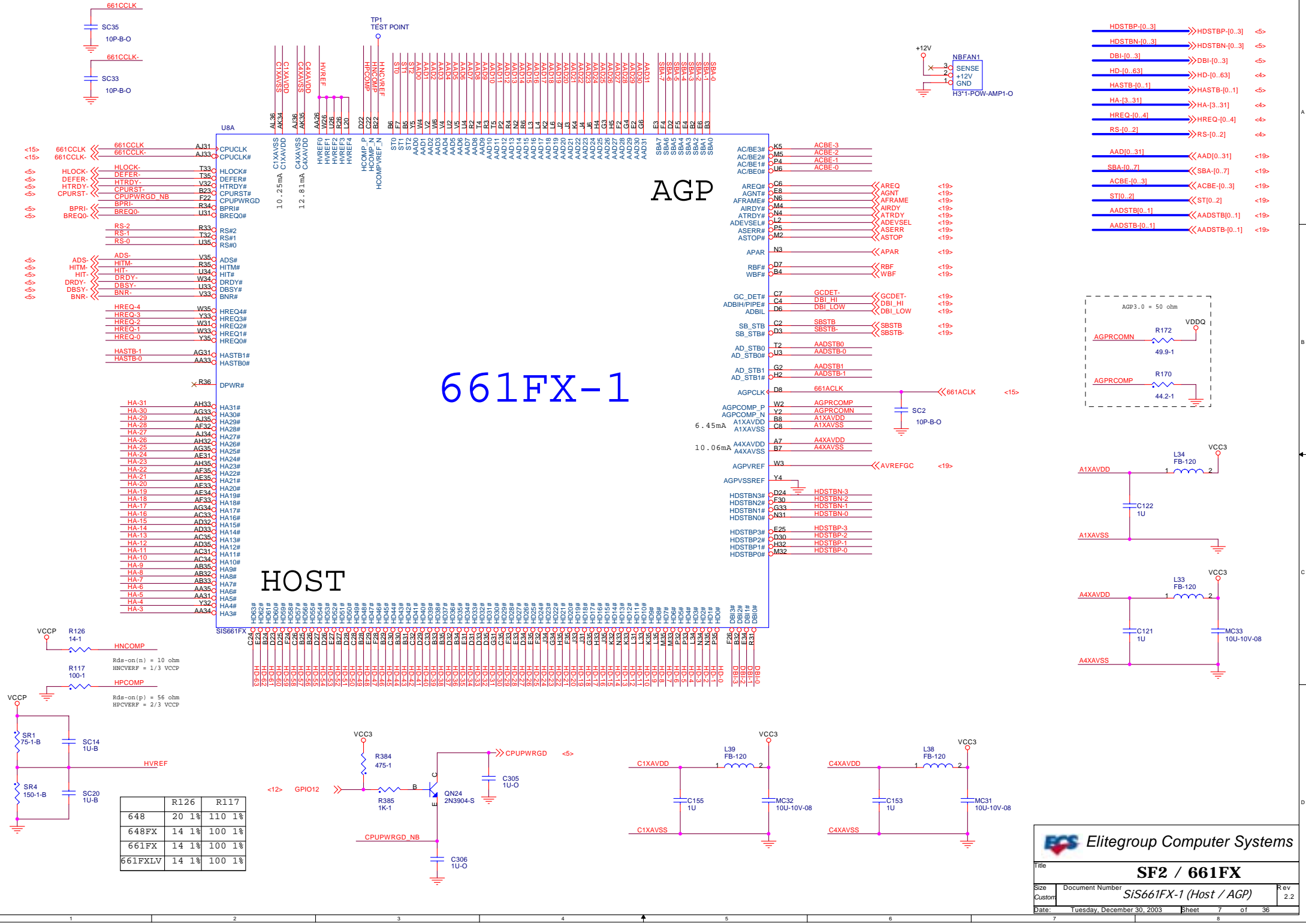
Put these capacitors at processor SOUTH SIDE



P.S. choose X7R/X5R components instead of Y5V for all 10uF_1206 capacitors on this page.

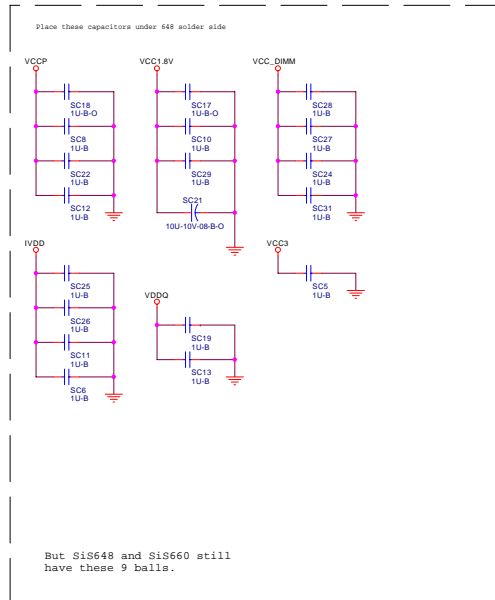
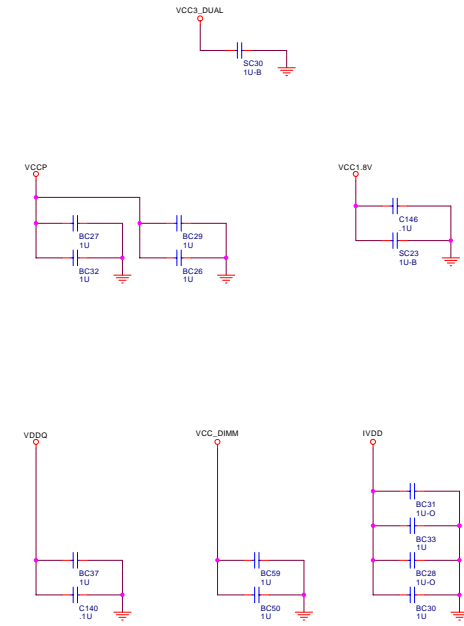
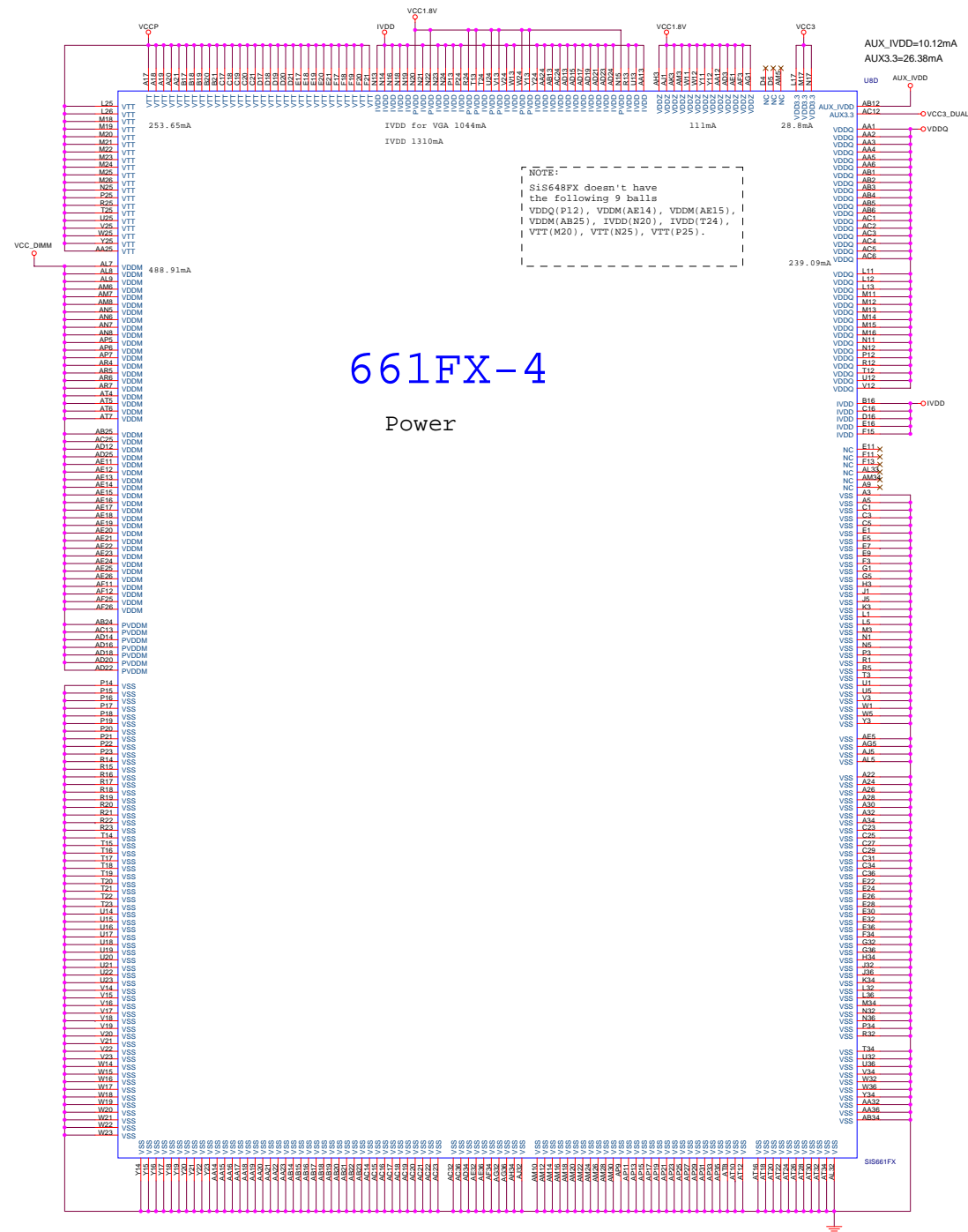
Put these capacitors at processor SOLDER SIDE

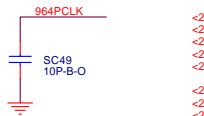
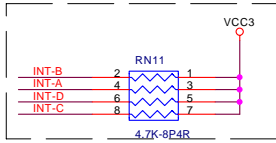




661FX-4

Power





<22,23,24,25> CBE[0..3]

<9,19,22,23> INT-A
<19,22,23,25> INT-B
<22,23,24> INT-C
<22,23> INT-D

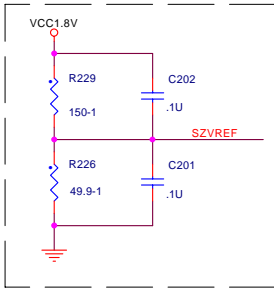
<22,23,24,25> FRAME-
<22,23,24,25> IRDY-
<22,23,24,25> TRDY-
<22,23,24,25> STOP-

<22,23,24> SERR-
<22,23,24,25> PAR
<22,23,24,25> DEVSEL-
<22,23> PLOCK-

<15> 964PCLK
<19,20,22,23,24,25> PCIRST-
<28> SIOPCIRST-
<9> NBCIRST-

<15> 964ZCLK
<9> ZSTB0
<9> ZSTB-0
<9> ZSTB1
<9> ZSTB-1

<9> ZUREQ
<9> ZDREQ



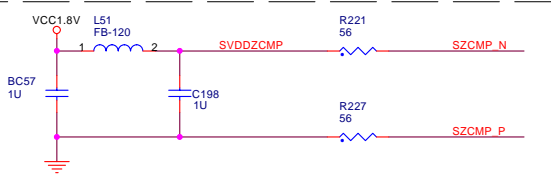
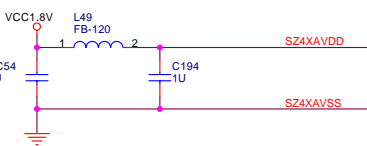
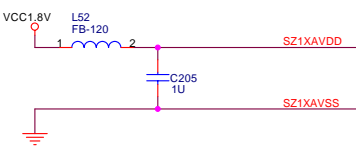
SZCMP_N AA24
SZCMP_P AA25

SZ1XAVDD AC26
SZ1XAVSS AB25
SZ4XAVDD Y22
SZ4XAVSS AA23

SZVREF AA26
ZAD16 Y26

<9> ZAD[0..16]

Analog Power supplies of Transzip function for 96X Chip.



PCI

IDE

964-1

HyperZip

ZAD0 ZAD1 ZAD2 ZAD3 ZAD4 ZAD5 ZAD6 ZAD7 ZAD8 ZAD9 ZAD10 ZAD11 ZAD12 ZAD13 ZAD14 ZAD15

W24 W25 W26 W27 W28 W29 W30 W31 W32 W33 W34 W35 W36 W37 W38 W39 W40 W41 W42 W43 W44 W45 W46 W47 W48 W49 W50 W51 W52 W53 W54 W55 W56 W57 W58 W59 W60 W61 W62 W63 W64 W65 W66 W67 W68 W69 W70 W71 W72 W73 W74 W75 W76 W77 W78 W79 W80 W81 W82 W83 W84 W85 W86 W87 W88 W89 W90 W91 W92 W93 W94 W95 W96 W97 W98 W99 W100

10mA IDEAVDD IDEAVSS

ICHRDYA AE15
IDREQA AC15
IIRQA AE16
CBLIDA AE16

IOIRAR AF15
IOIWAR AC14
IDACKAR AD15

IDCSA1 AF17
IDCSA0 AF17

ICHRDYB AE22
IDREQB AC22
IIRQB AE23
CBLIDB AE23

IOIRBR AF22
IOIWRB AC21
IDACKBR AD22

IDCSA2 AF24
IDCSA1 AF23
IDCSA0 AD23

IDCSB1 AF25
IDCSB0 AF24

IDA0 AF14
IDA1 AF13
IDA2 AF13
IDA3 AF12
IDA4 AF11
IDA5 AF11
IDA6 AF10
IDA7 AF10
IDA8 AE11
IDA9 AC11
IDA10 AE12
IDA11 AE12
IDA12 AC12
IDA13 AE13
IDA14 AC13
IDA15 AE14

IDB0 AF21
IDB1 AD20
IDB2 AF20
IDB3 AD19
IDB4 AF19
IDB5 AD18
IDB6 AF18
IDB7 AD17
IDB8 AF17
IDB9 AE18
IDB10 AC18
IDB11 AE19
IDB12 AC19
IDB13 AE20
IDB14 AC20
IDB15 AE21

IDEDA0 AE14
IDEDA1 AF13
IDEDA2 AF13
IDEDA3 AF12
IDEDA4 AF11
IDEDA5 AF11
IDEDA6 AF10
IDEDA7 AF10
IDEDA8 AE11
IDEDA9 AC11
IDEDA10 AE12
IDEDA11 AE12
IDEDA12 AC12
IDEDA13 AE13
IDEDA14 AC13
IDEDA15 AE14

IDEDB0 AF21
IDEDB1 AD20
IDEDB2 AF20
IDEDB3 AD19
IDEDB4 AF19
IDEDB5 AD18
IDEDB6 AF18
IDEDB7 AD17
IDEDB8 AF17
IDEDB9 AE18
IDEDB10 AC18
IDEDB11 AE19
IDEDB12 AC19
IDEDB13 AE20
IDEDB14 AC20
IDEDB15 AE21

IDEDA0 AE14
IDEDA1 AF13
IDEDA2 AF13
IDEDA3 AF12
IDEDA4 AF11
IDEDA5 AF11
IDEDA6 AF10
IDEDA7 AF10
IDEDA8 AE11
IDEDA9 AC11
IDEDA10 AE12
IDEDA11 AE12
IDEDA12 AC12
IDEDA13 AE13
IDEDA14 AC13
IDEDA15 AE14

IDEDB0 AF21
IDEDB1 AD20
IDEDB2 AF20
IDEDB3 AD19
IDEDB4 AF19
IDEDB5 AD18
IDEDB6 AF18
IDEDB7 AD17
IDEDB8 AF17
IDEDB9 AE18
IDEDB10 AC18
IDEDB11 AE19
IDEDB12 AC19
IDEDB13 AE20
IDEDB14 AC20
IDEDB15 AE21

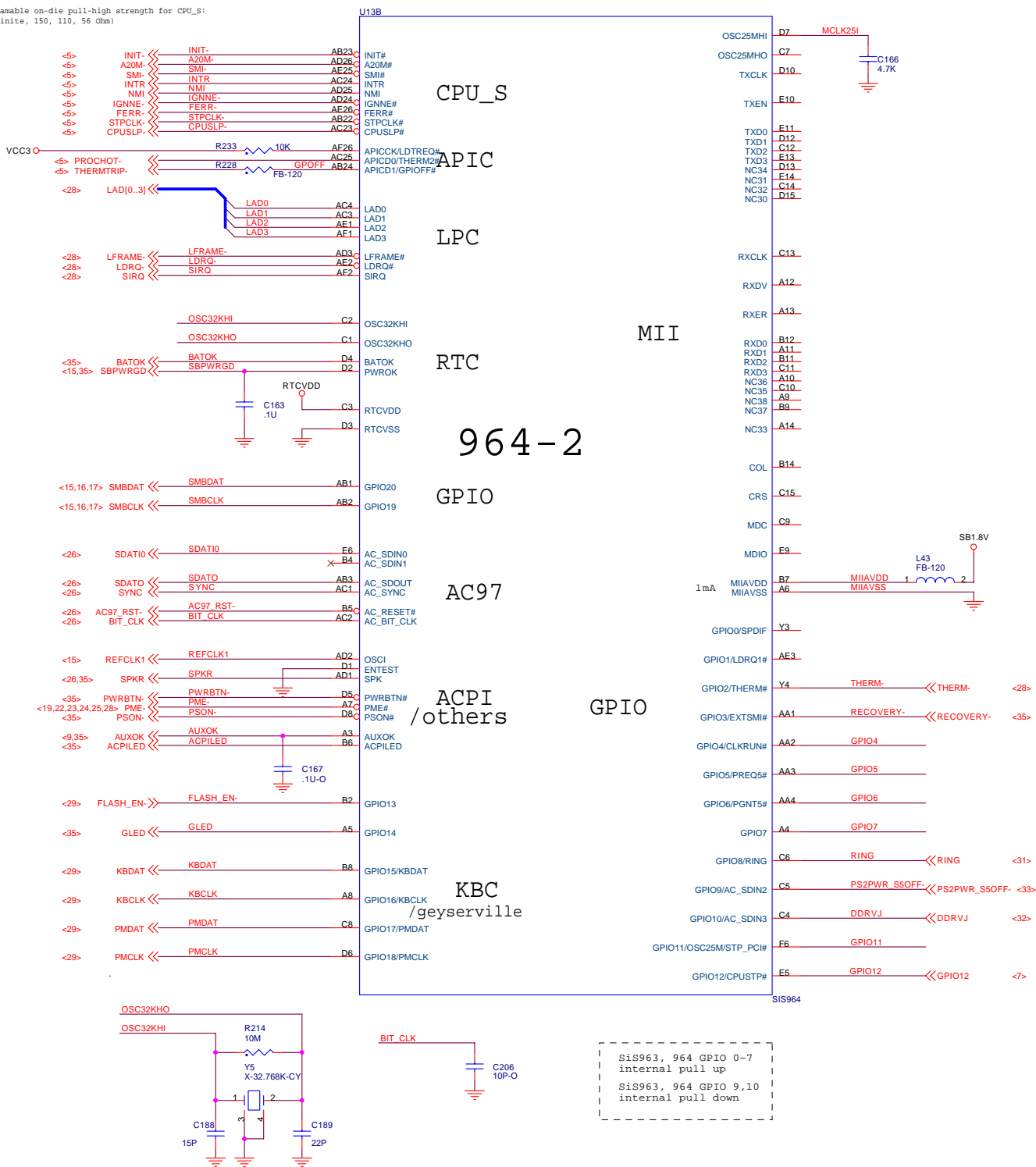
SIS964

Elitegroup Computer Systems

SF2 / 661FX

Size Document Number SIS964-1 (PCI / IDE / Link) Rev 2.2

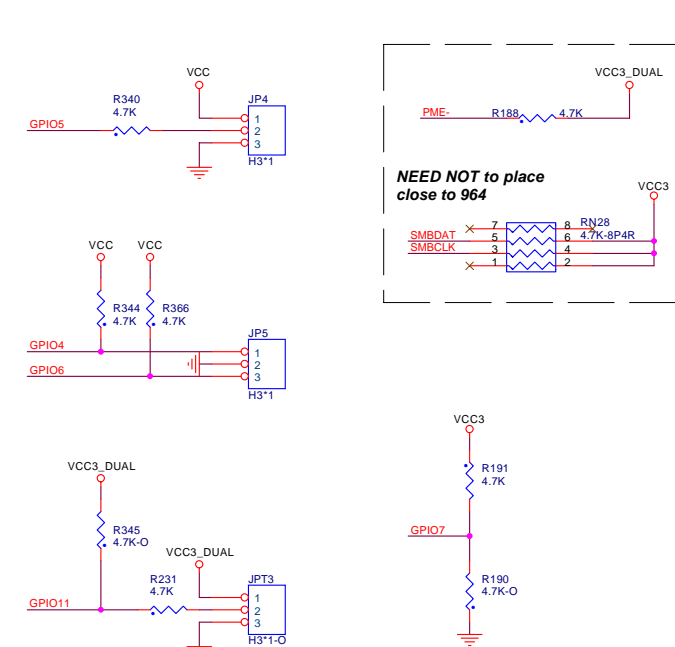
Date: Monday, December 29, 2003 Sheet 11 of 36

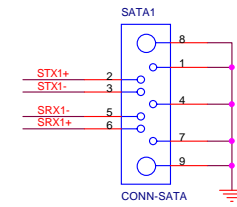
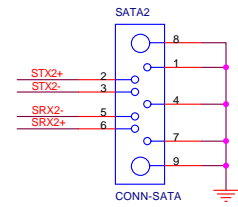
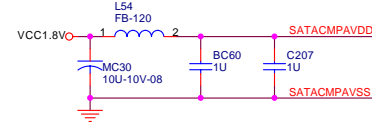
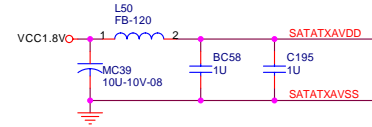
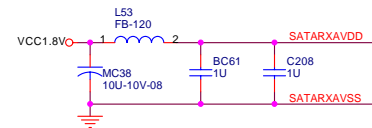
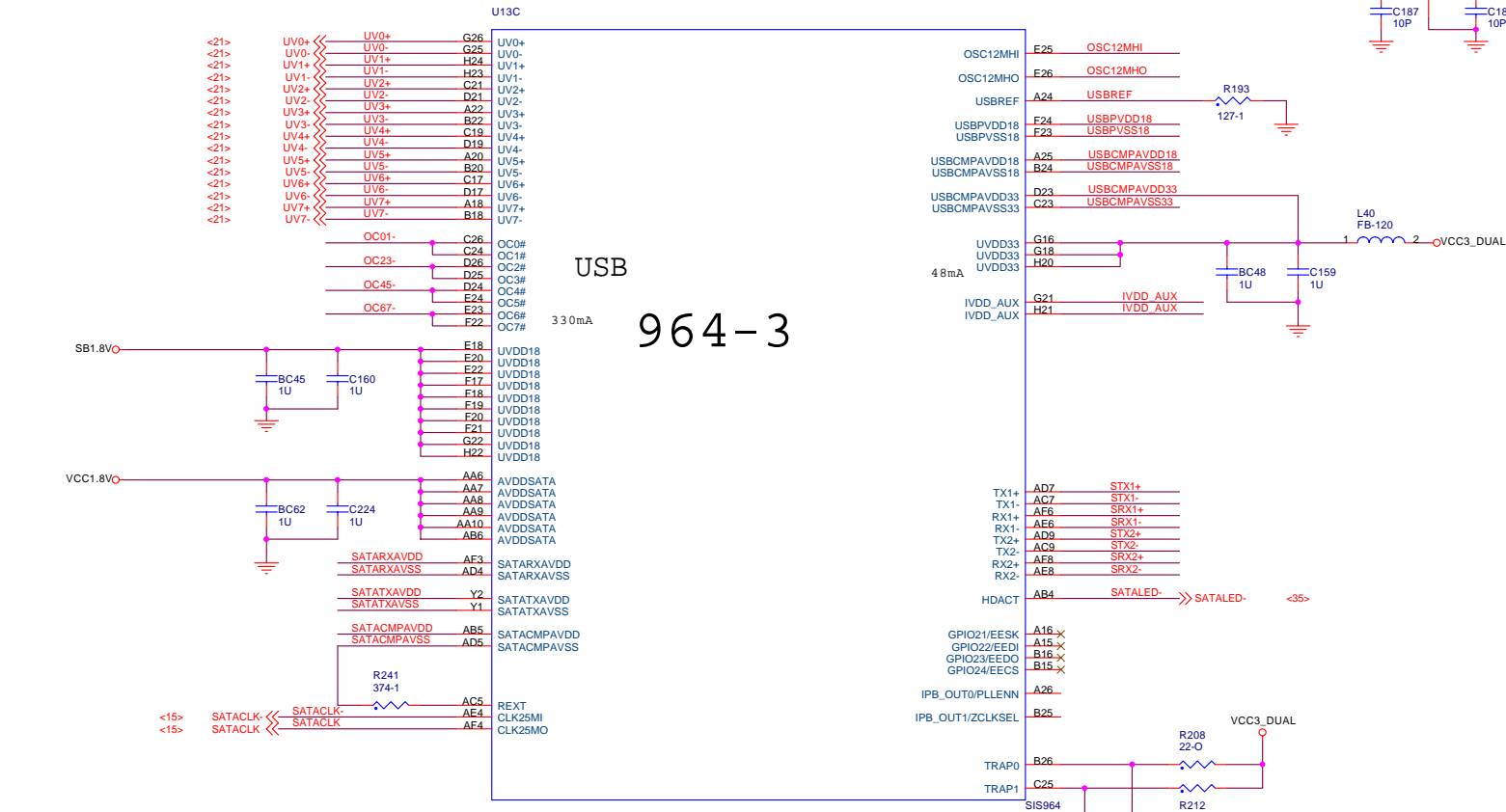
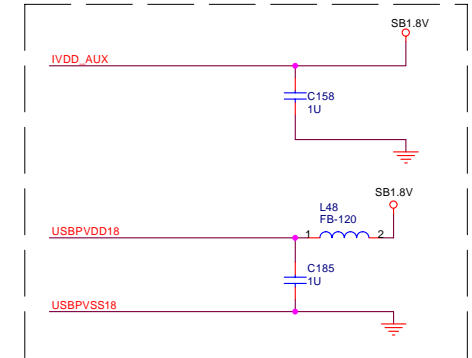
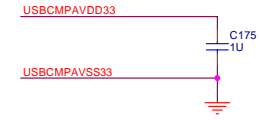
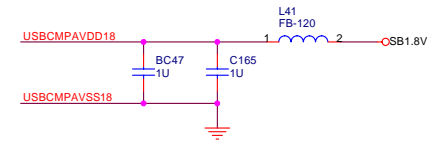
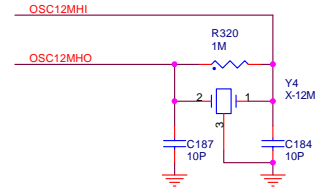
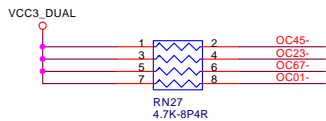


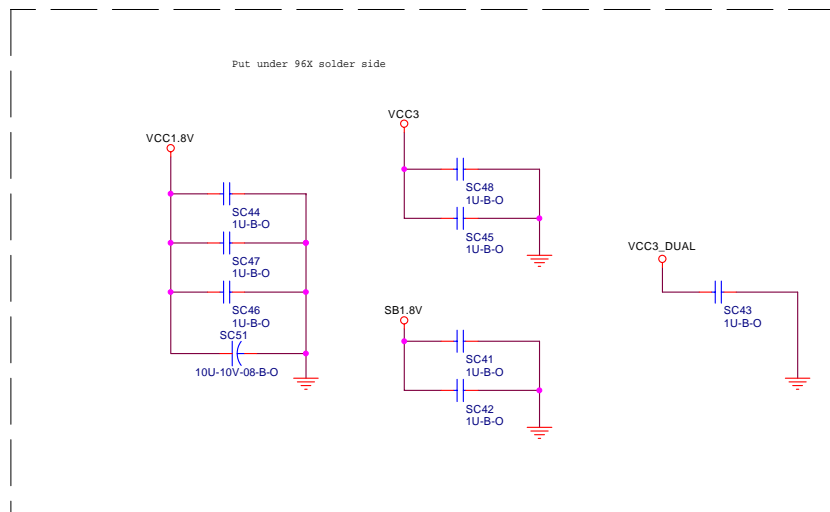
JP4		1-2	2-3
GPIO5		1	0
HP	Clear CMOS	Normal	Clear
TRIGEM	Suspen Mode	S1 & S3	S1

JP5		1-2	2-3	Open
(GPIO4, GPIO6)		(0, 1)	(1, 0)	(1, 1)
HP	Clear Password	Normal	Clear	/
TRIGEM	BIOS Logo	TG	Commaeul	No Logo

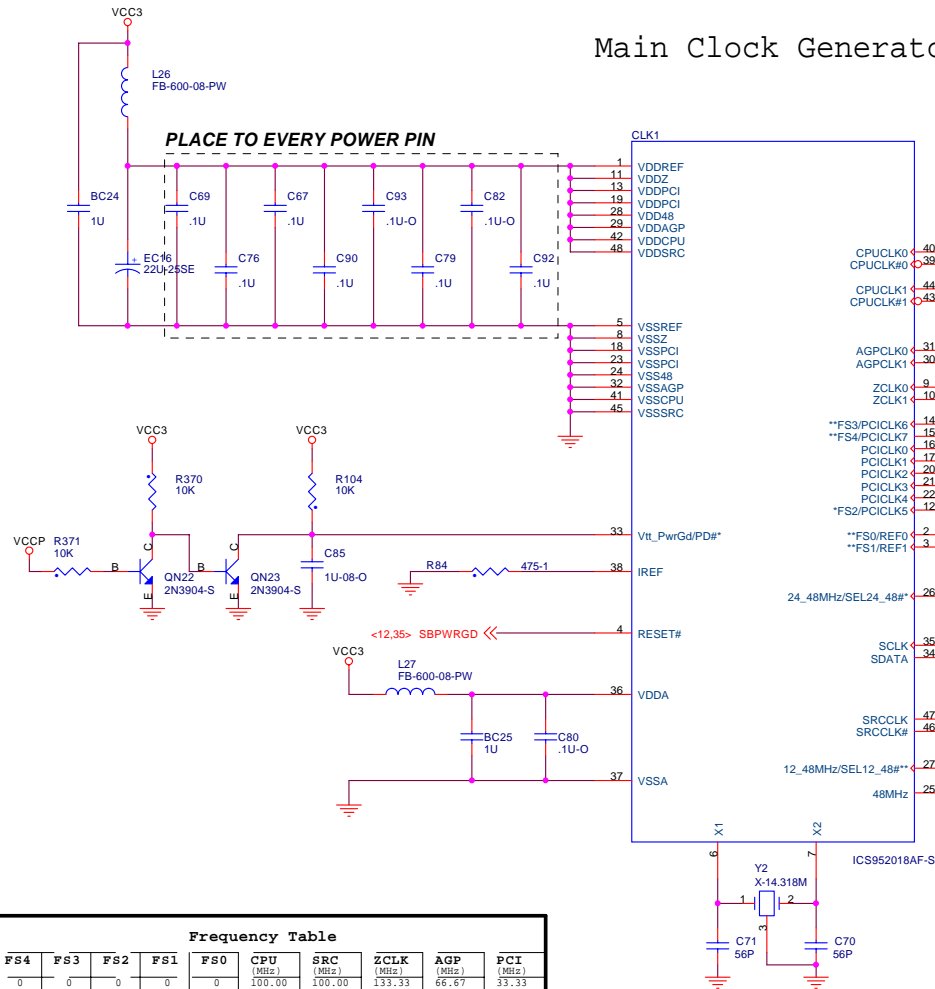
<i>JPT3</i>	<i>1-2</i>	<i>2-3</i>
GPI011	1	0
<i>Reserved</i>	-	-



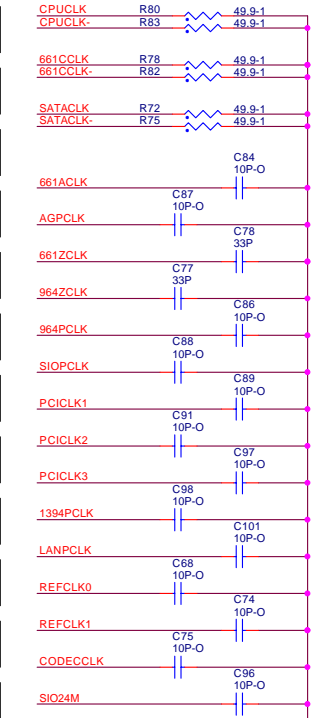




Main Clock Generator



By-Pass Capacitors Place near to the Clock Outputs



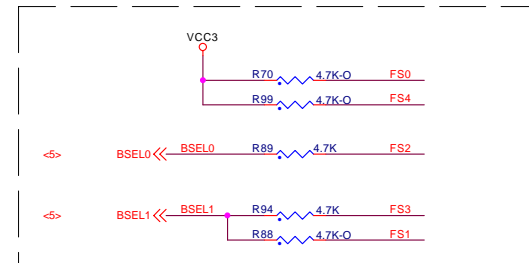
Frequency Table

FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SRC (MHz)	ZCLK (MHz)	AGP (MHz)	PCI (MHz)
0	0	0	0	0	100.00	100.00	133.33	66.67	33.33
0	0	0	0	1	100.99	100.99	134.65	67.33	33.66
0	0	0	1	0	103.00	103.00	137.33	68.67	34.33
0	0	0	1	1	100.00	100.00	133.33	66.67	33.33
0	0	1	0	0	133.33	100.00	133.33	66.66	33.33
0	0	1	0	1	134.65	100.99	134.65	67.32	33.66
0	0	1	1	0	137.33	103.00	137.33	68.66	34.33
0	0	1	1	1	133.33	100.00	133.33	66.67	33.33
0	1	0	0	0	200.00	100.00	133.33	66.67	33.33
0	1	0	0	1	201.98	100.99	134.65	67.33	33.66
0	1	0	1	0	206.00	103.00	137.33	68.67	34.33
0	1	0	1	1	200.00	100.00	133.33	66.67	33.33
0	1	1	0	0	166.66	125.00	125.00	66.66	33.33
0	1	1	0	1	168.31	126.23	126.23	67.32	33.66
0	1	1	1	0	171.66	128.74	128.74	68.66	34.33
0	1	1	1	1	166.66	125.00	125.00	66.66	33.33

Frequency Table

FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SRC (MHz)	ZCLK (MHz)	AGP (MHz)	PCI (MHz)
1	0	0	0	0	105.00	105.00	140.00	70.00	35.00
1	0	0	0	1	107.00	107.00	142.67	71.33	35.67
1	0	0	1	0	109.00	109.00	145.33	72.67	36.33
1	0	0	1	1	110.00	110.00	146.67	73.33	36.67
1	0	1	0	0	140.00	105.00	140.00	70.00	35.00
1	0	1	0	1	142.66	107.00	142.67	71.33	35.67
1	0	1	1	0	145.33	109.00	145.33	72.66	36.33
1	0	1	1	1	146.66	110.00	146.66	73.33	36.67
1	1	0	0	0	210.00	105.00	140.00	70.00	35.00
1	1	0	0	1	214.00	107.00	142.67	71.33	35.67
1	1	0	1	0	218.00	109.00	145.33	72.67	36.33
1	1	0	1	1	220.00	110.00	146.67	73.33	36.67
1	1	1	0	0	266.66	100.00	133.33	66.67	33.33
1	1	1	0	1	269.33	101.00	134.67	67.33	33.67
1	1	1	1	0	274.66	103.00	137.33	68.67	34.33
1	1	1	1	1	266.66	100.00	133.33	66.67	33.33

Frequency Selection



Clock Generator Table	FS4	FS3	FS2	FS1	FS0
Hardware Trapping	Low	BSEL1	BSEL0	Low	Low
CPU=100 (BSEL[1:0]=00)	0	0	0	0	0
CPU=133 (BSEL[1:0]=01)	0	0	1	0	0
CPU=200 (BSEL[1:0]=10)	0	1	0	0	0

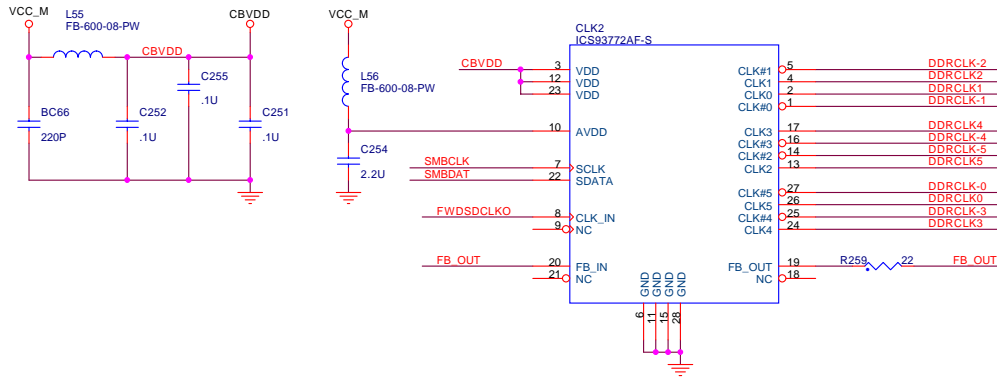
Elitegroup Computer Systems

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Size	Document Number	Main Clock	Rev 2.2
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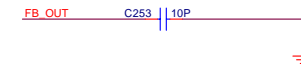
Clock Buffer (DDR)

(5 OPTIONS)
 1: (ICS) ICS93716
 2: (Winbond)
 3: (ICWorks)
 4: (IMI)
 5: (AMI)

By-Pass Capacitors
 Place near to the Clock Buffer



DDRCLK[0..5] <<DDRCLK[0..5] <17>
 DDRCLK[0..5] <<DDRCLK[0..5] <17>
 SMBCLK <<SMBCLK <12,15,17>
 SMBDAT <<SMBDAT <12,15,17>
 FWSDCLKO <<FWSDCLKO <8>

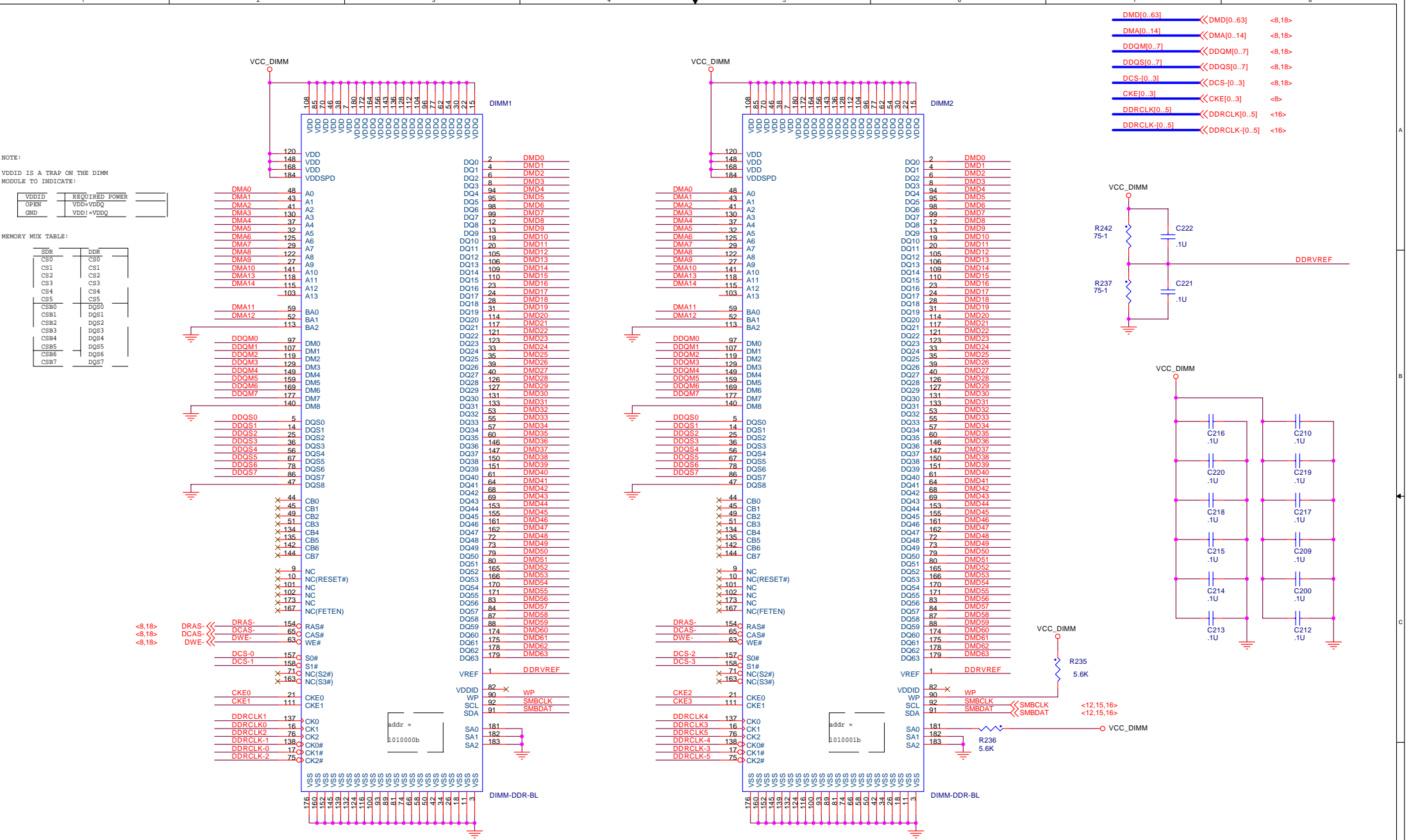


NOTE:
VDDID IS A TRAP ON THE DIMM
MODULE TO INDICATE:

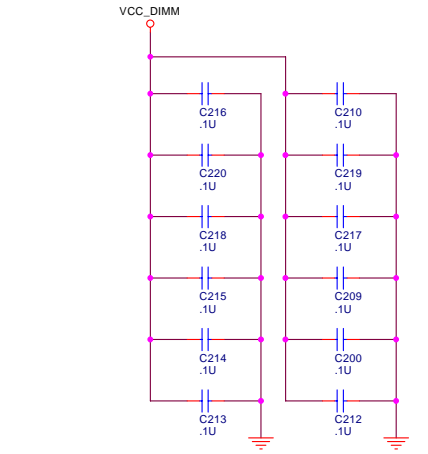
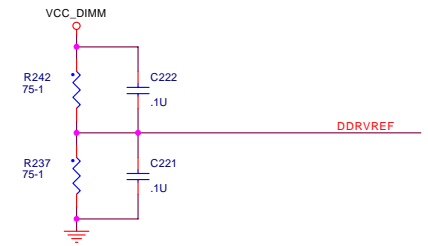
VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDDI+=VDDQ

MEMORY MUX TABLE:

SDR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	CSB0
CSB1	CSB1
CSB2	CSB2
CSB3	CSB3
CSB4	CSB4
CSB5	CSB5
CSB6	CSB6
CSB7	CSB7



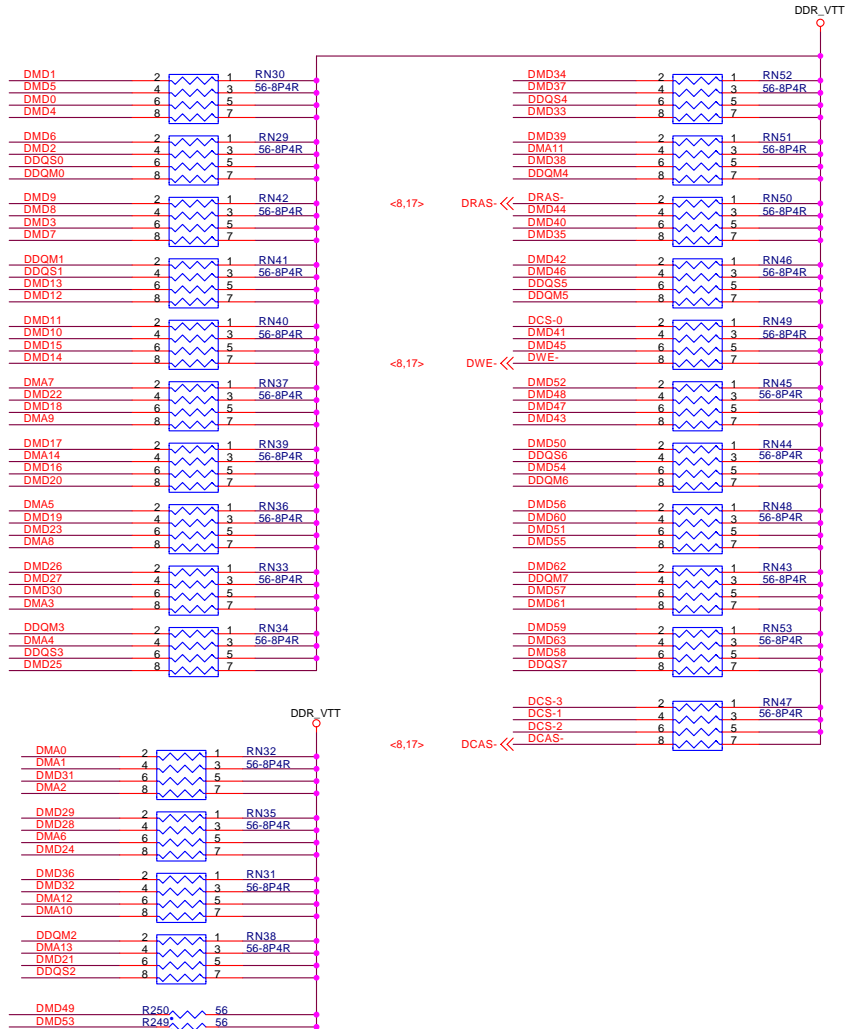
- DMD[0..63] << DMD[0..63] <-8,18>
- DMA[0..14] << DMA[0..14] <-8,18>
- DDQM[0..7] << DDQM[0..7] <-8,18>
- DDQS[0..7] << DDQS[0..7] <-8,18>
- DCS[0..3] << DCS[0..3] <-8,18>
- CKE[0..3] << CKE[0..3] <-8>
- DDRCLK[0..5] << DDRCLK[0..5] <-16>
- DDRCLK[0..5] << DDRCLK[0..5] <-16>



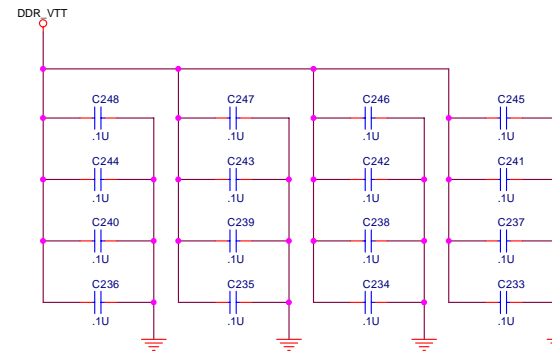
SSTL-2 Termination Resistors

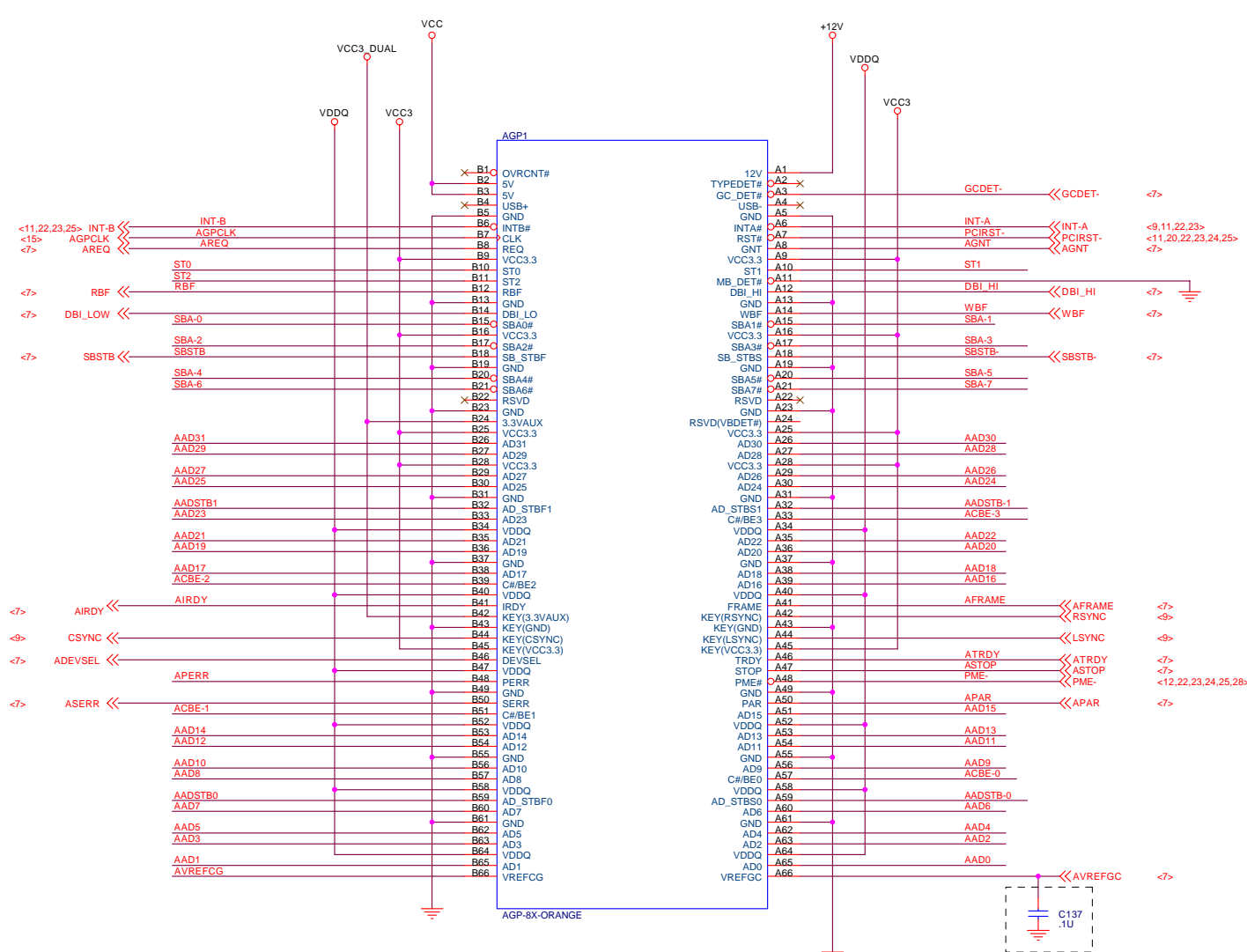
	DDR		DDR		DDR		Rtt
MD/DQM (/DQS)	LV-CMOS	Ra	SSTL-2	Ra	1.0	B3	
MA/Control	LV-CMOS	0/10/-	SSTL-2	0	0	B3	
CS	LV-CMOS	0	SSTL-2	0	0	47	
CKE	0D 3.3V		DD 2.5V				

DMD[0..63]	<<DMD[0..63]	<8,17>
DMA[0..14]	<<DMA[0..14]	<8,17>
DDQM[0..7]	<<DDQM[0..7]	<8,17>
DDQS[0..7]	<<DDQS[0..7]	<8,17>
DCS-[0..3]	<<DCS-[0..3]	<8,17>



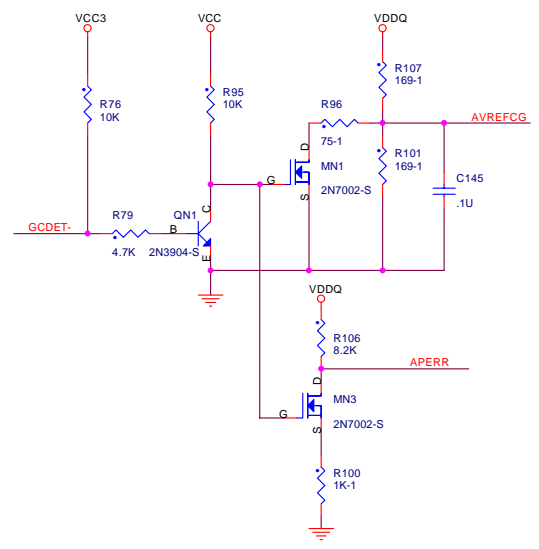
DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND
0603 Package placed within 200mils of VTT Termination R-packs



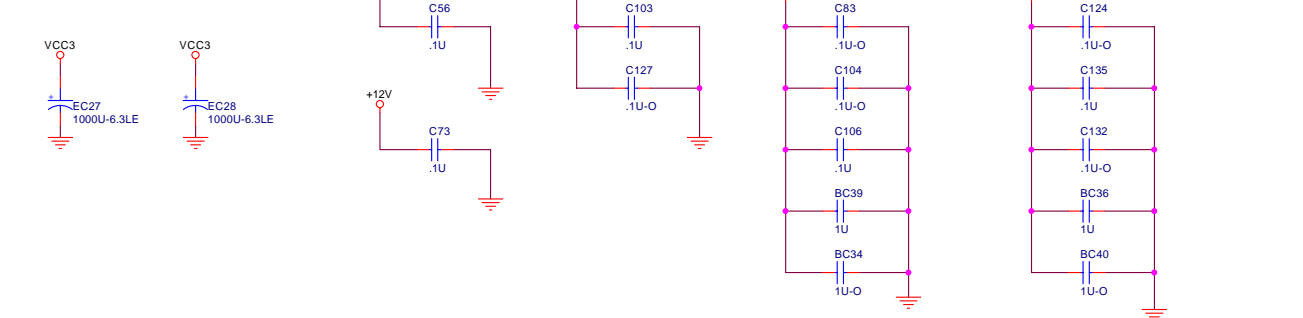


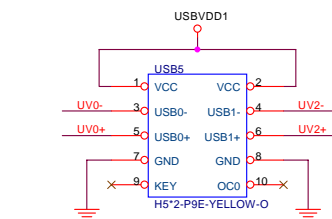
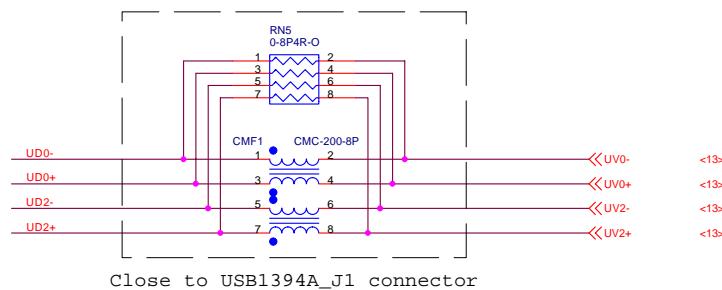
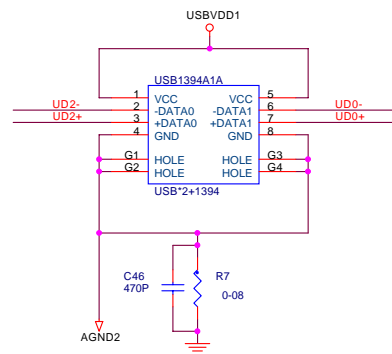
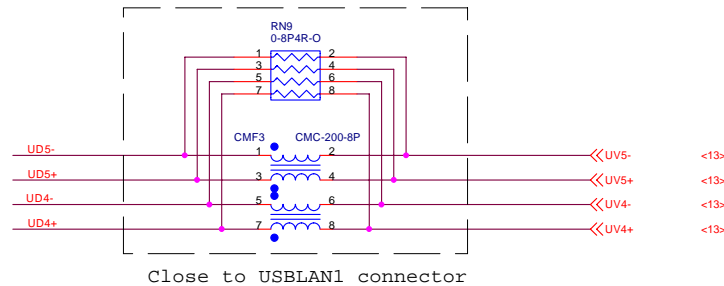
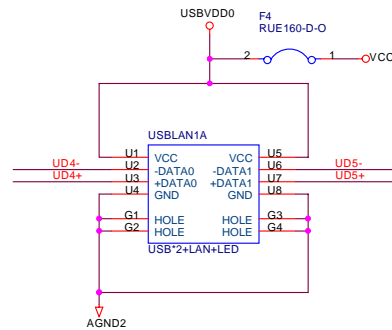
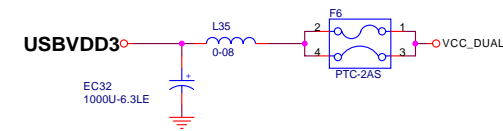
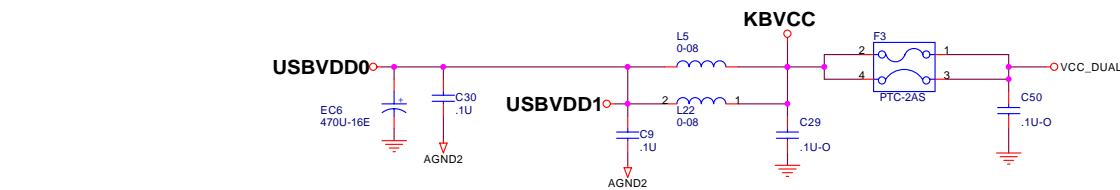
<7> SBA[0..7] << SBA[0..7]
 <7> ST[0..2] << ST[0..2]
 <7> ACBE[0..3] << ACBE[0..3]
 <7> AAD[0..31] << AAD[0..31]
 <7> AADSTB[0..1] << AADSTB[0..1]
 <7> AADSTB[0..1] << AADSTB[0..1]

GCDET-	Low	Hi
Graphic Card	AGP 3.0	AGP 2.0
AVREFCG	0.35	0.75
APERR	0	1.5

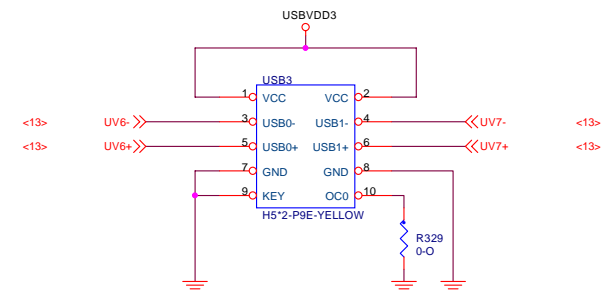
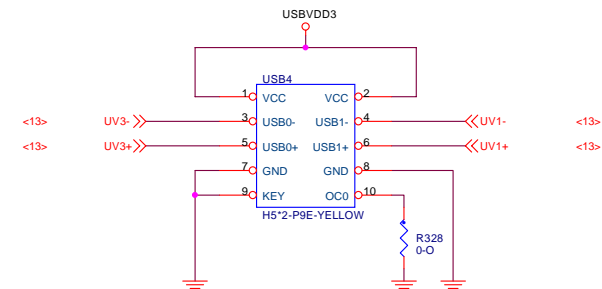


AGP CONNECTOR DECOUPLING
 put CAP close to AGP slot each POWER PIN

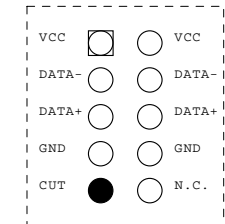




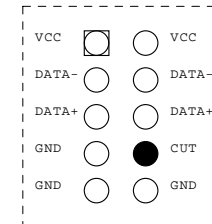
	USB port
Control 0	0, 3, 6
Control 1	1, 4, 7
Control 2	2, 5



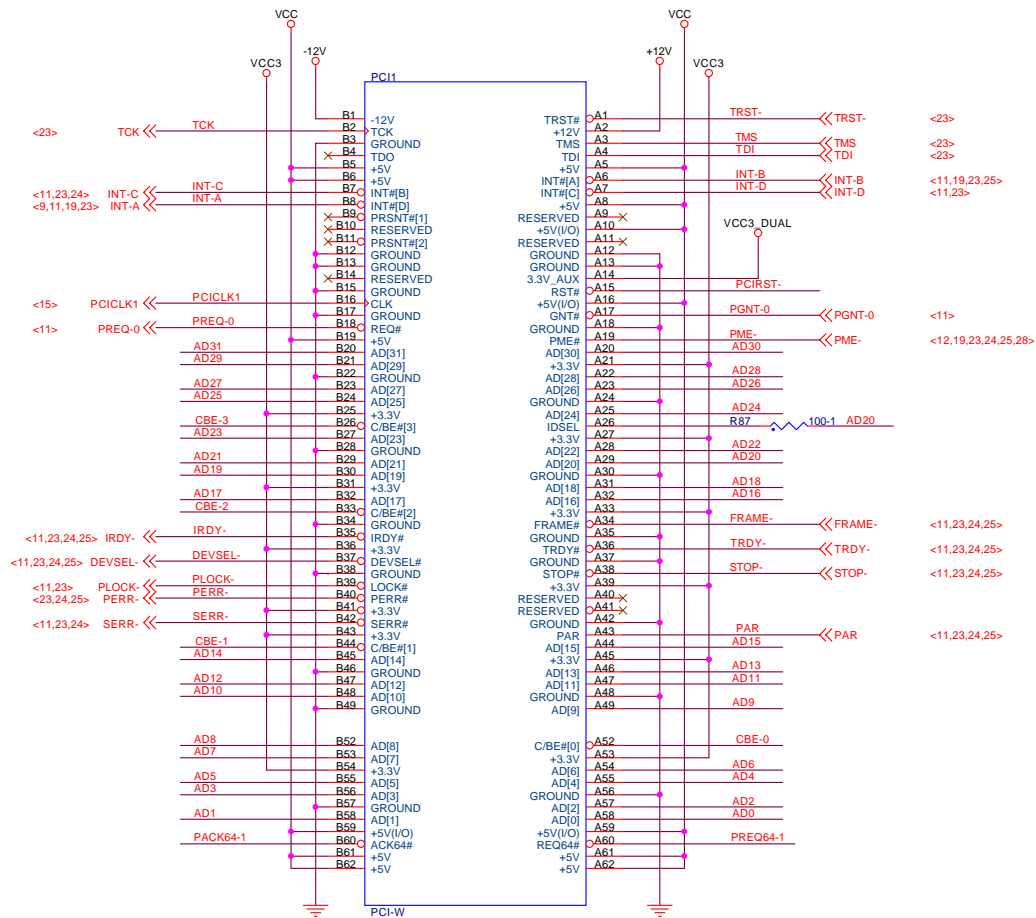
Intel USB Header



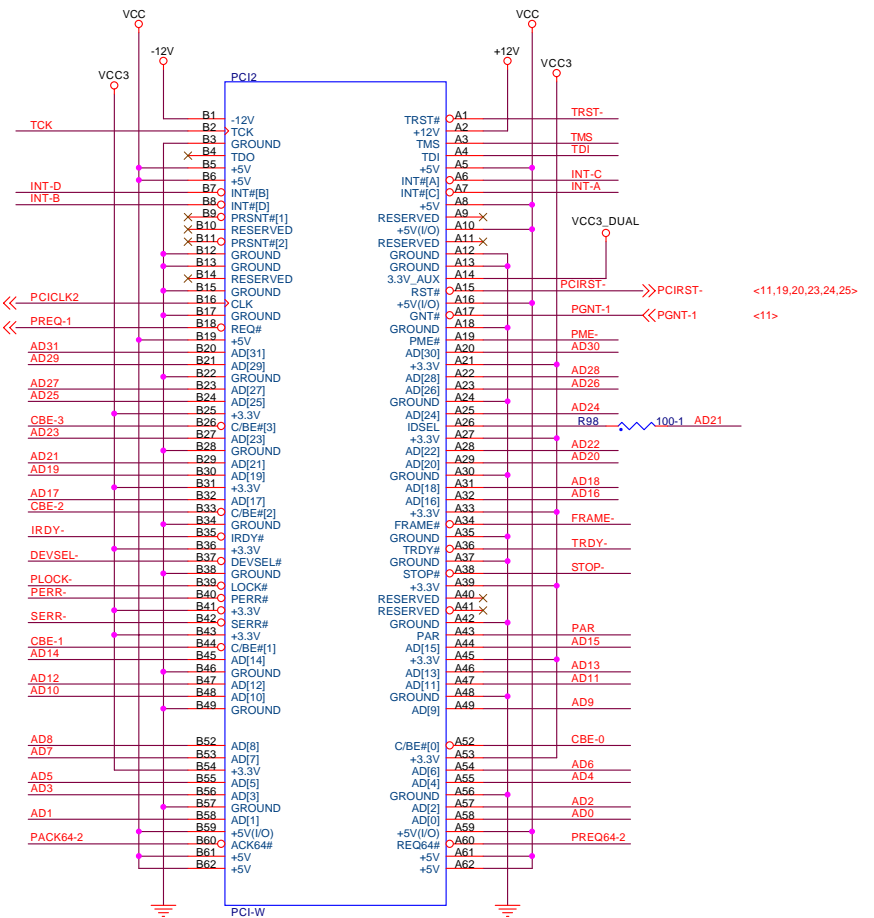
ACER USB Header



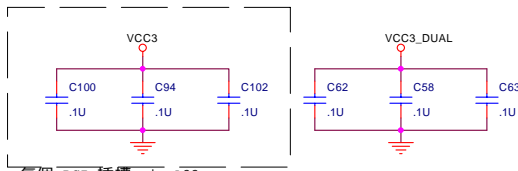
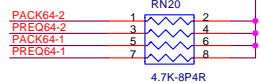
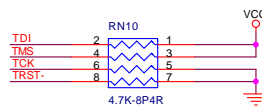
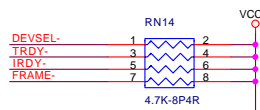
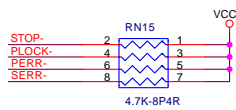
PCI Slot 1 & 2



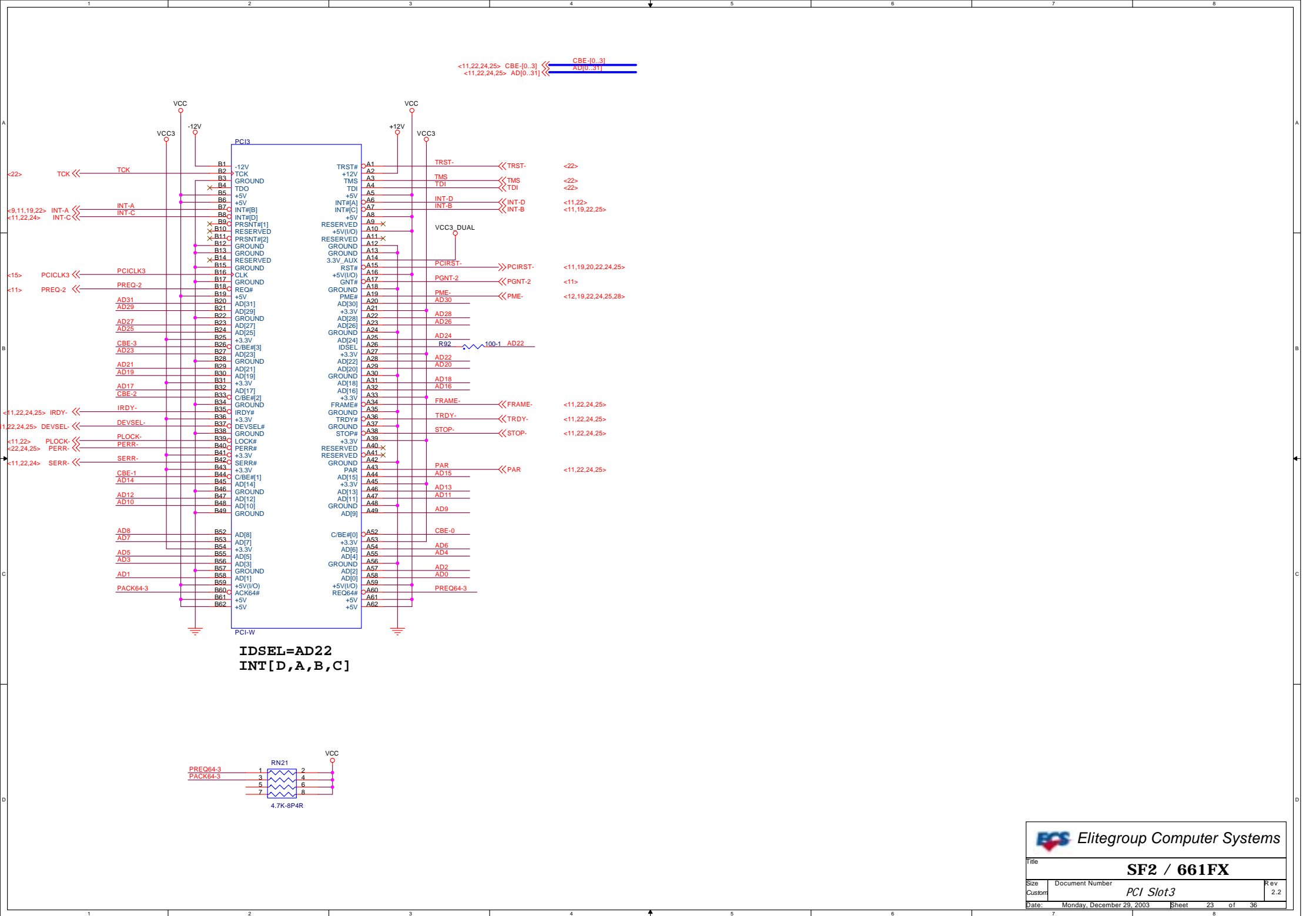
IDSSEL=AD20
INT[B,C,D,A]

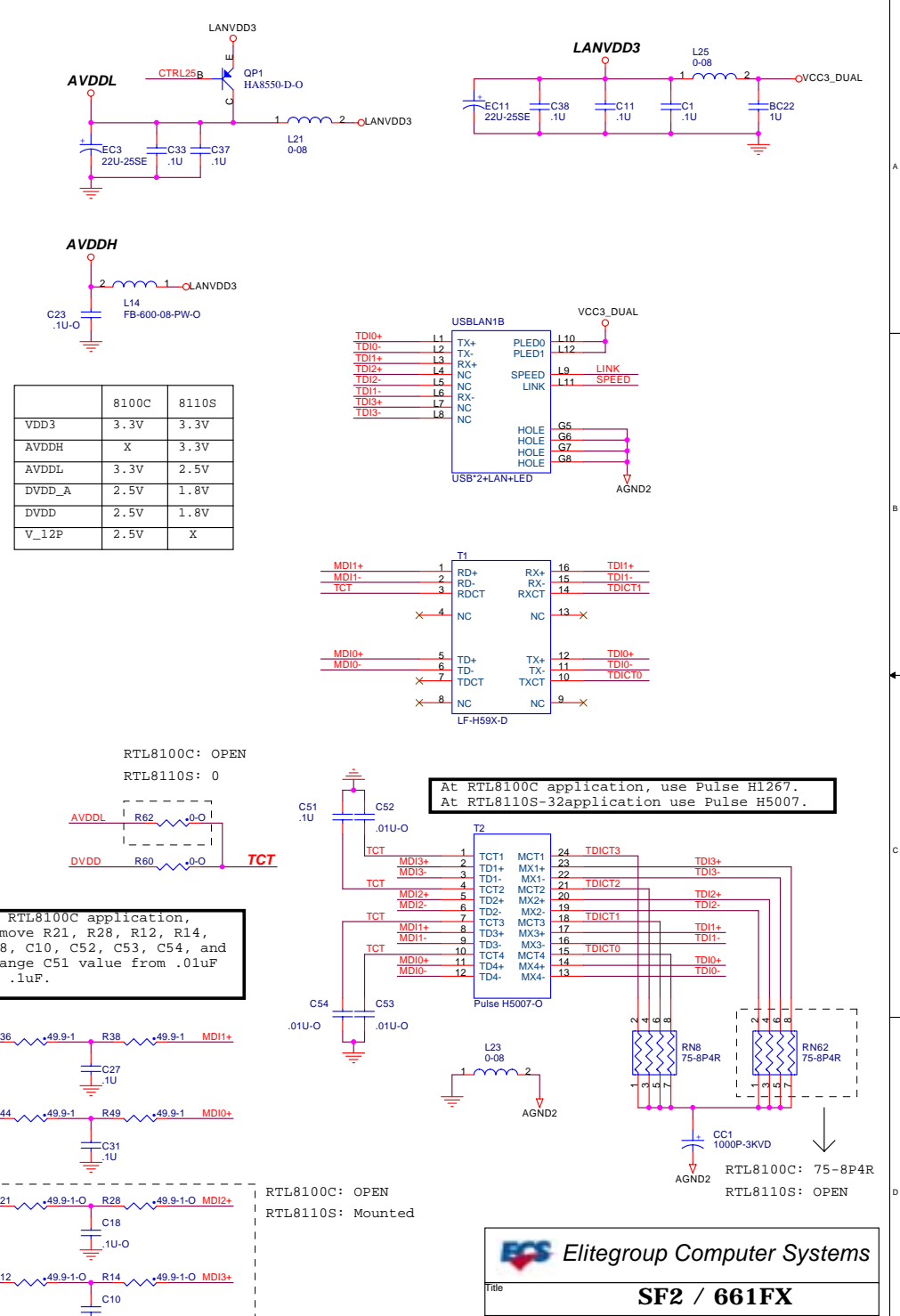
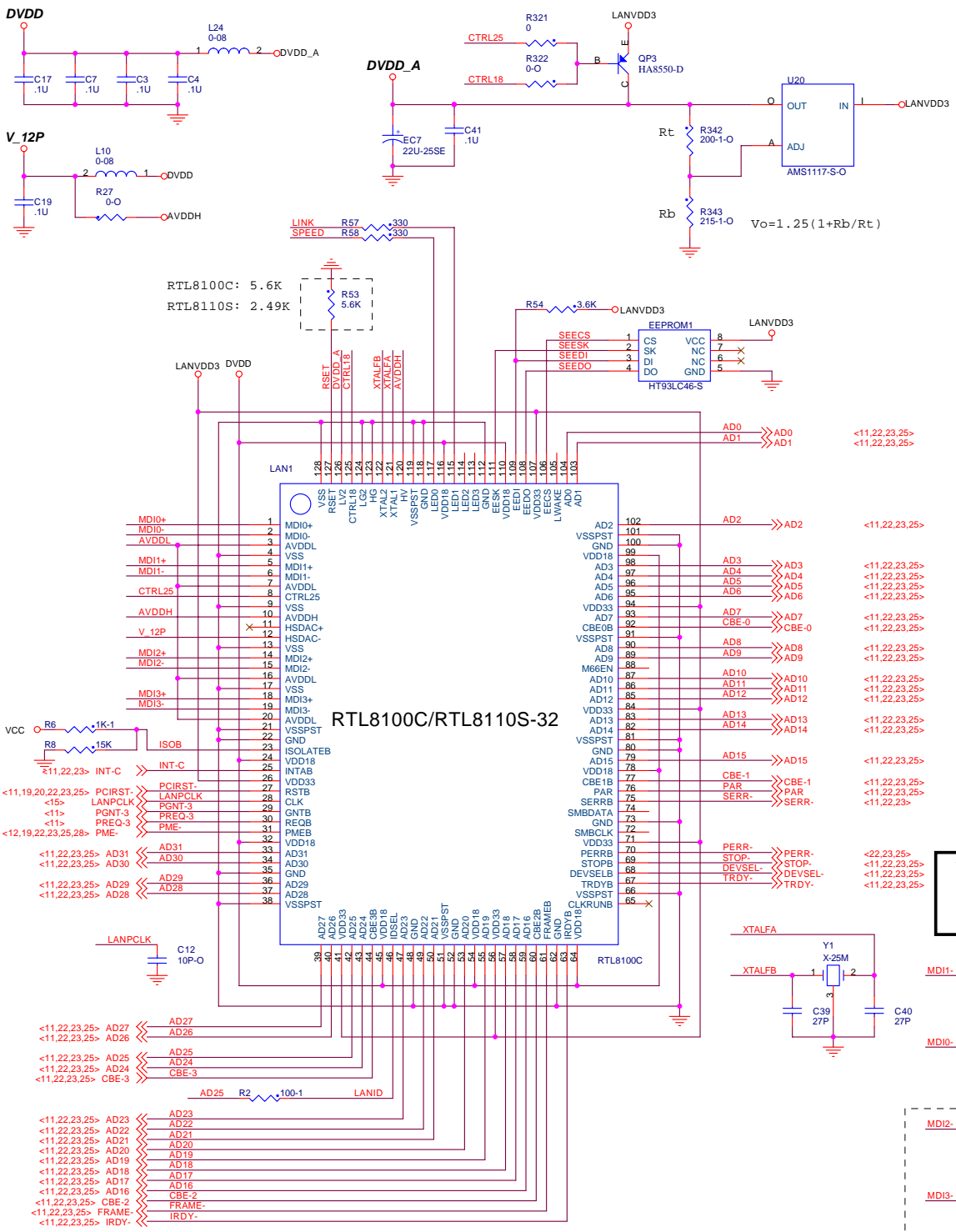


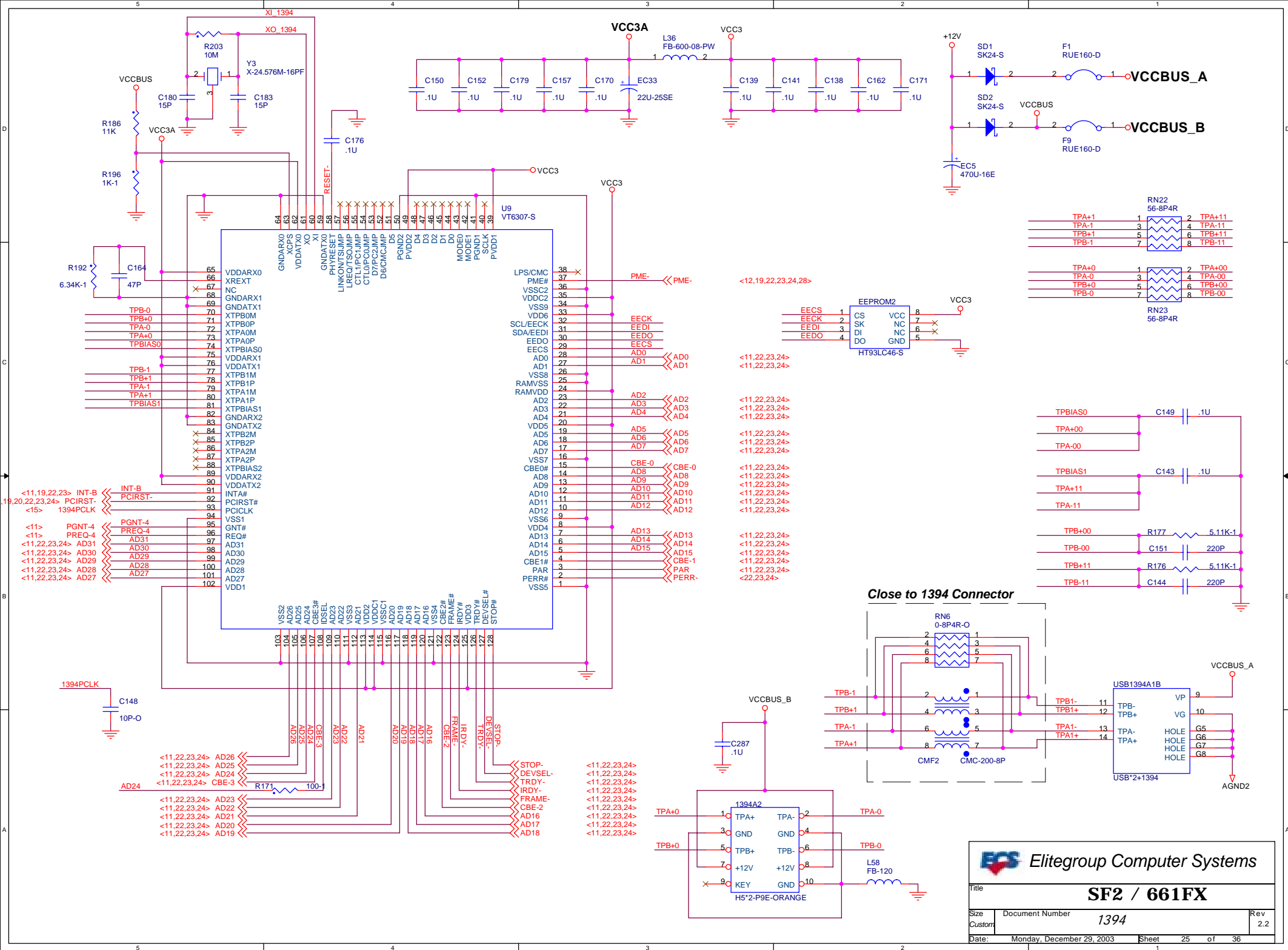
IDSSEL=AD21
INT[C,D,A,B]

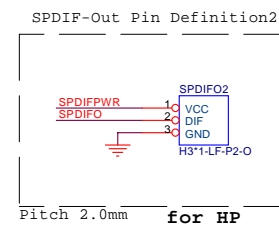
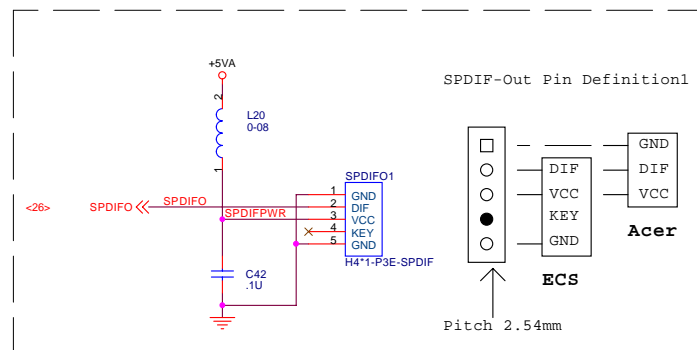
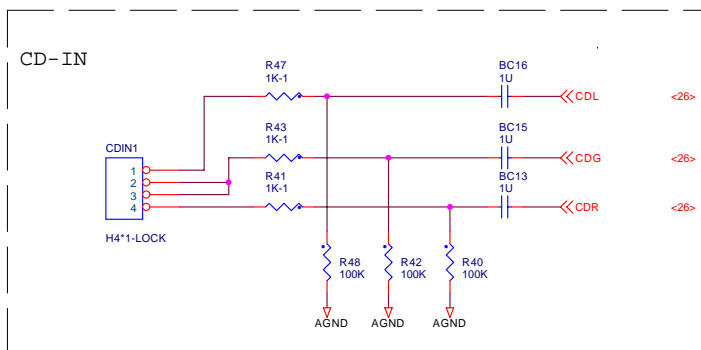
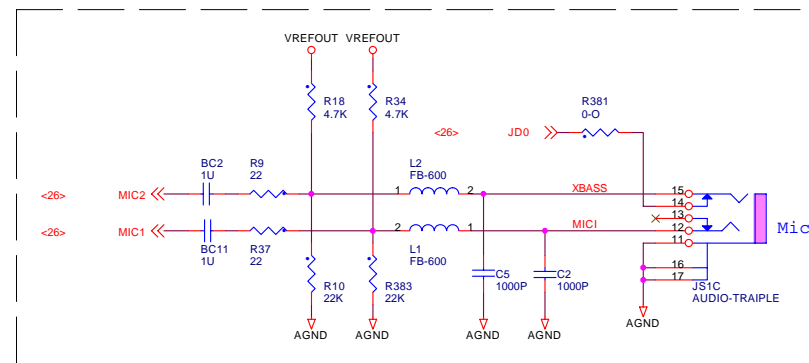
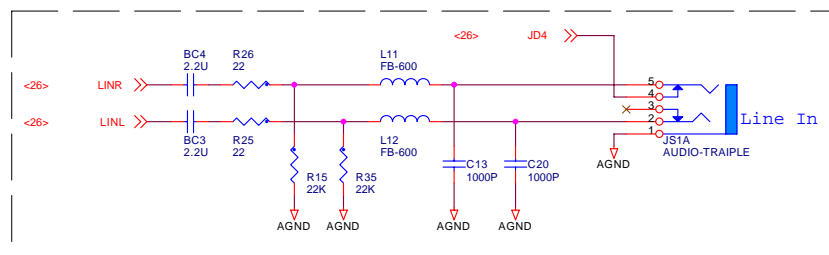
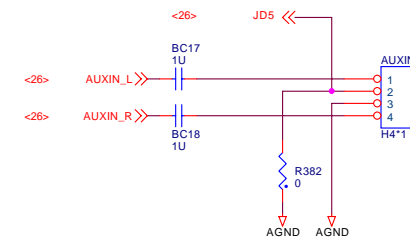
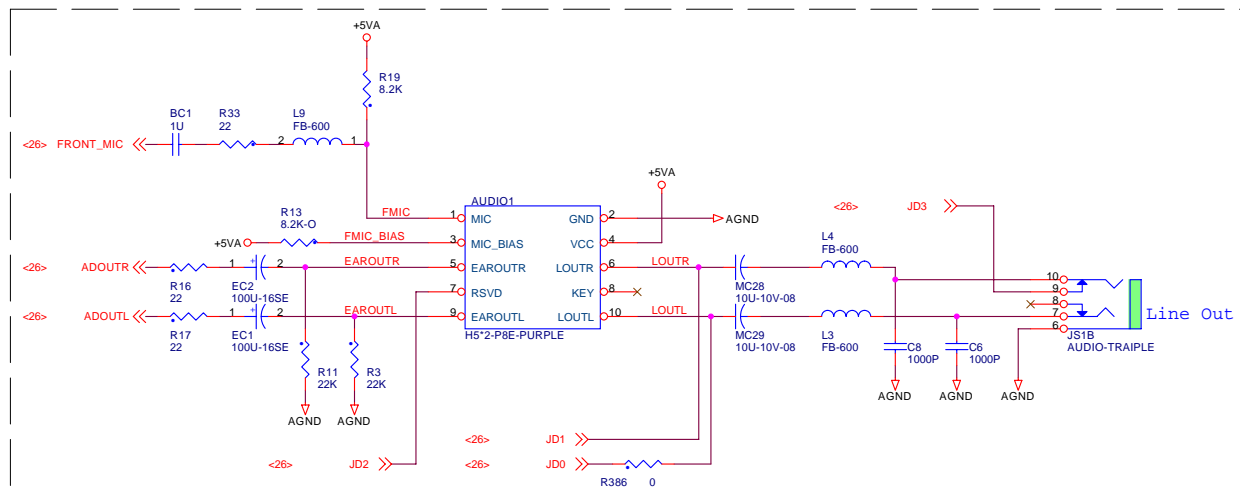


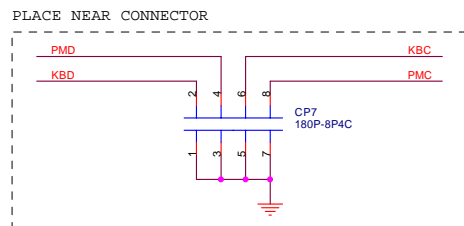
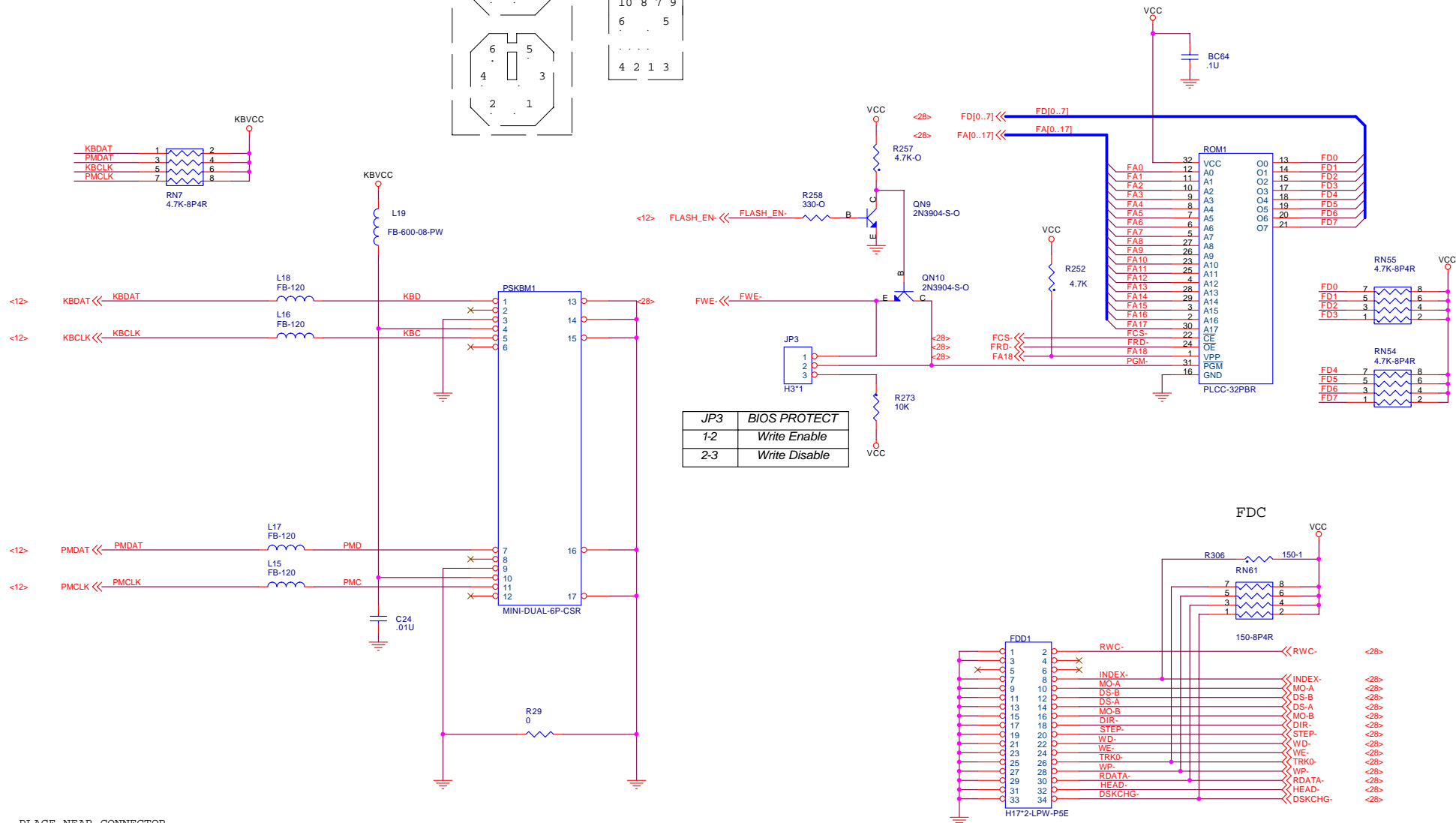
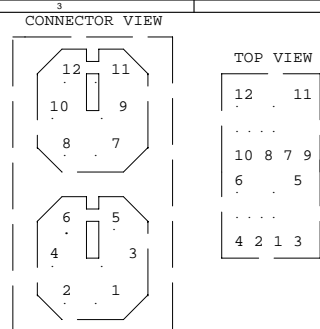
每個 PCI 插槽 pin A33
各放一顆

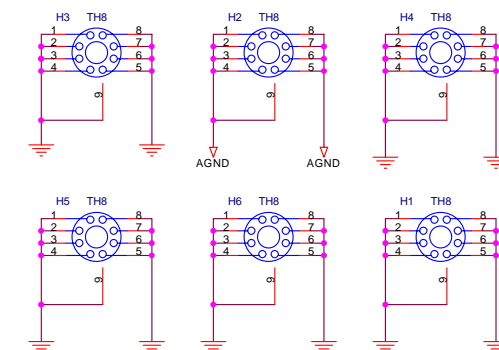
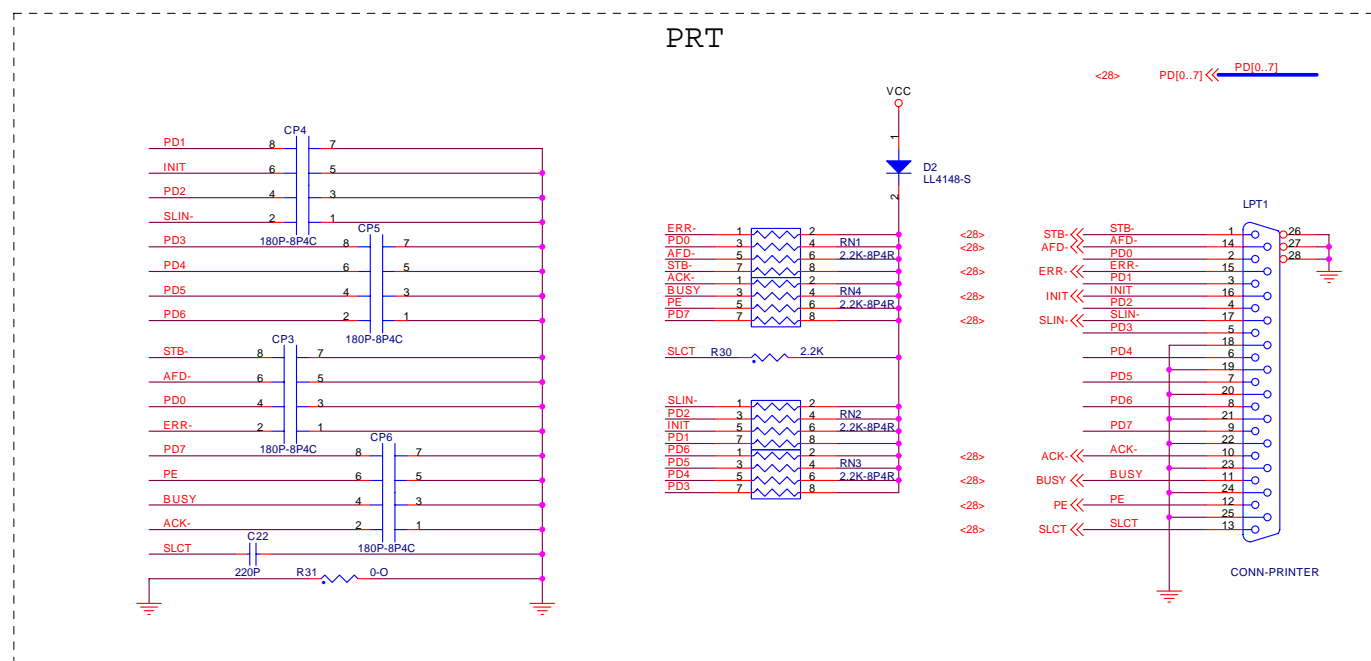
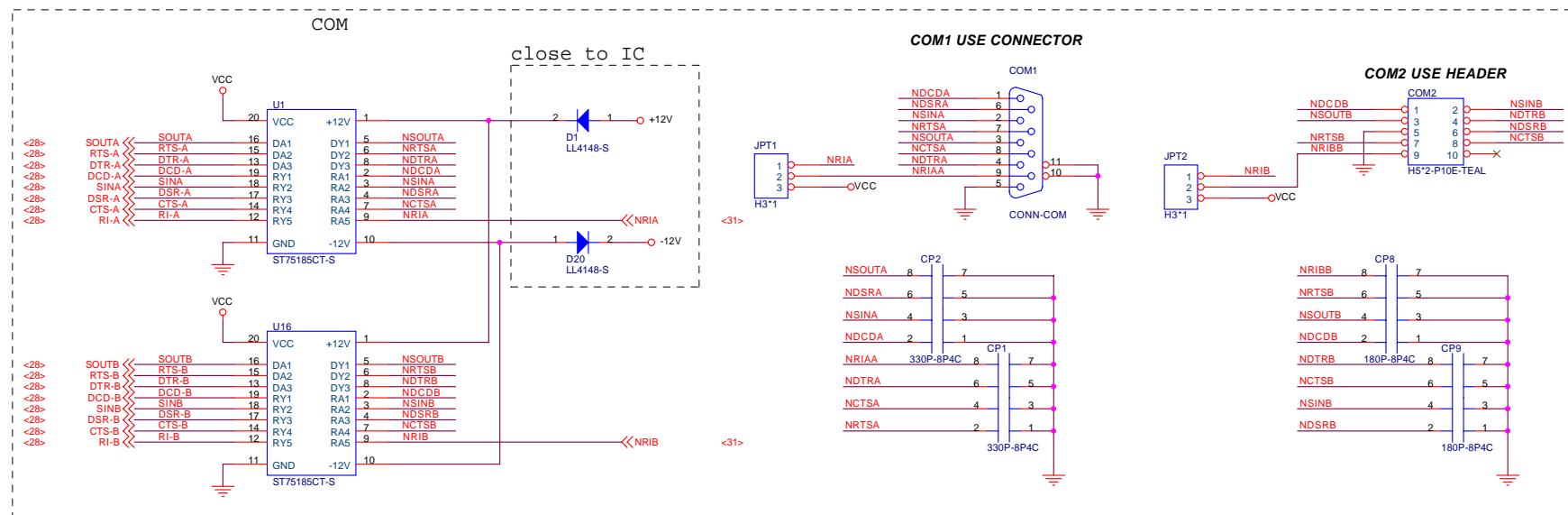






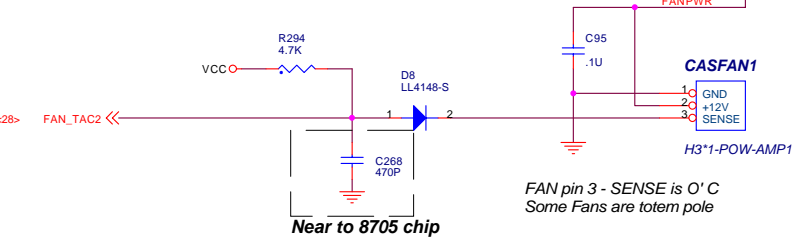
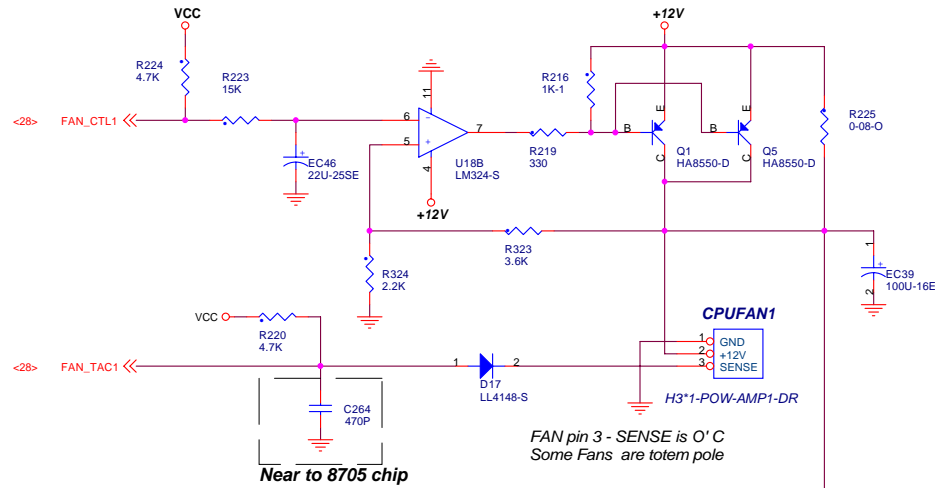




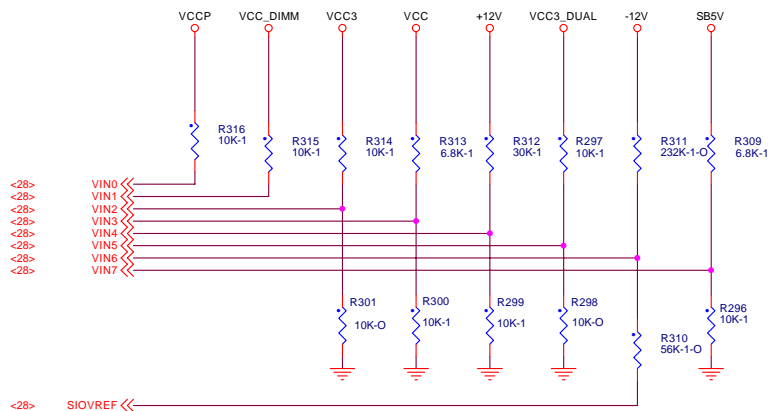


Layout :

Power Signals : CPUFAN, CASEFAN, PWFAN trace width should > 20 mil with current 200 mA .

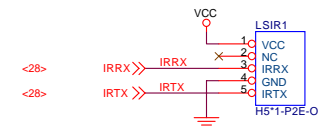
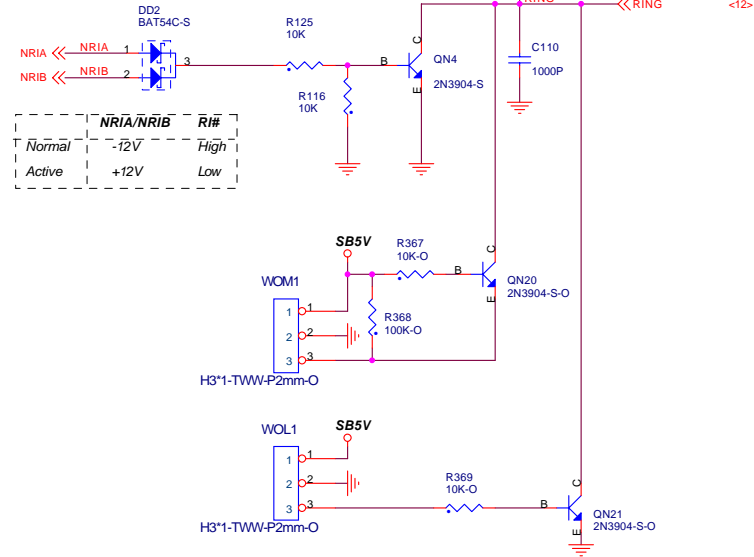
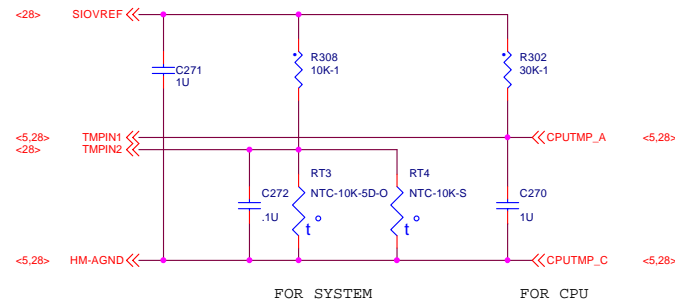


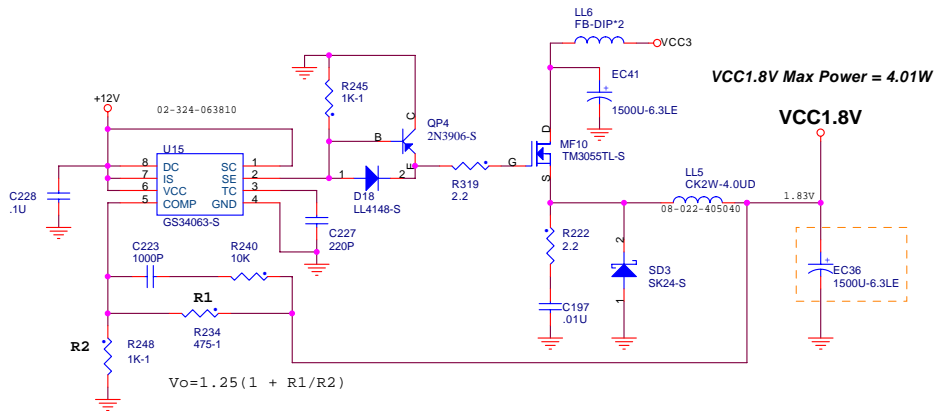
Voltage Monitor



Temperature Monitor

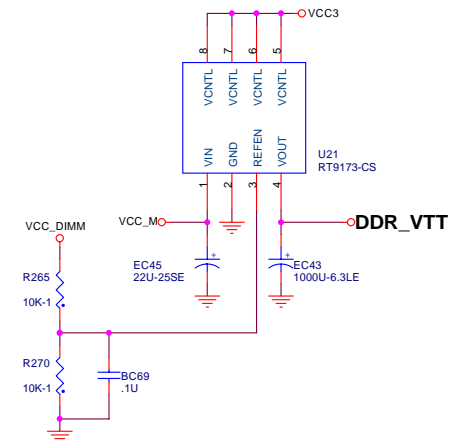
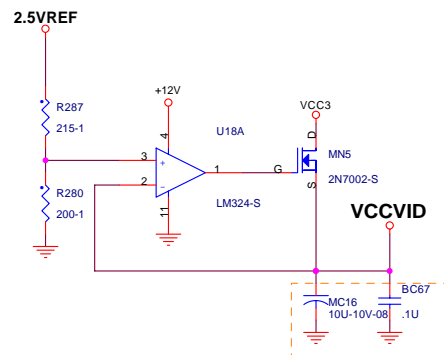
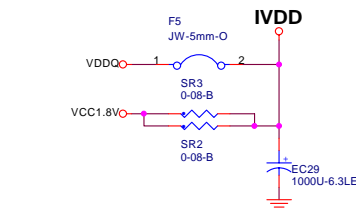
Choosing method of measuring temperature by either thermistor or diode



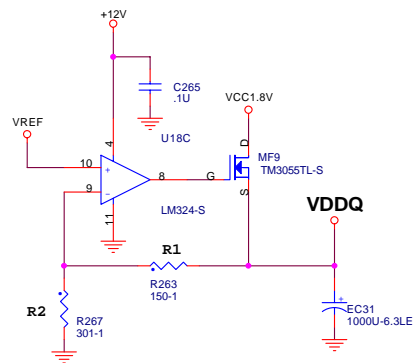


	IVDD	VCC1.8V	
648	1.8V	1.8V	short two power plane, one regulator
648FX	1.9V	1.9V	short two power plane, one regulator
661FX	1.8V	1.8V	short two power plane, one regulator or two regulator
661FXLV	1.5V	1.8V	two regulator

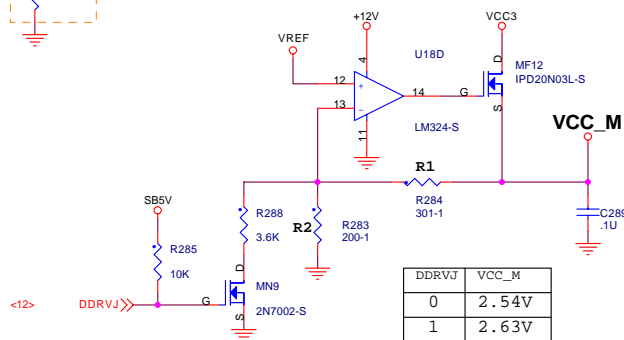
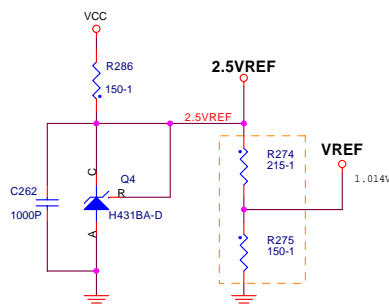
	AUX_IVDD	SB1.8V	
648	1.8V	1.8V	short two power plane, one regulator
648FX	1.9V	1.9V	short two power plane, one regulator
661FX	1.8V	1.8V	short two power plane, one regulator
661FXLV	1.5V	1.8V	two regulator



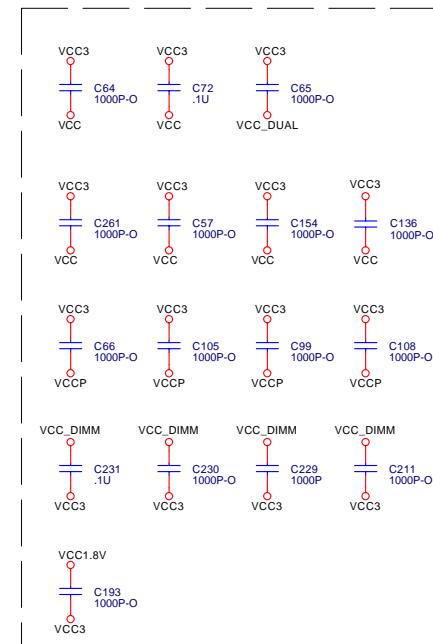
VCC1.5V Max Power = 0.3*(0.289+2.35)=0.7917W



$$V_o = V_{REF}(1 + R_1/R_2)$$



DDRVJ	VCC_M
0	2.54V
1	2.63V



平均分布在POWER PLAN 和 PLAN 之間

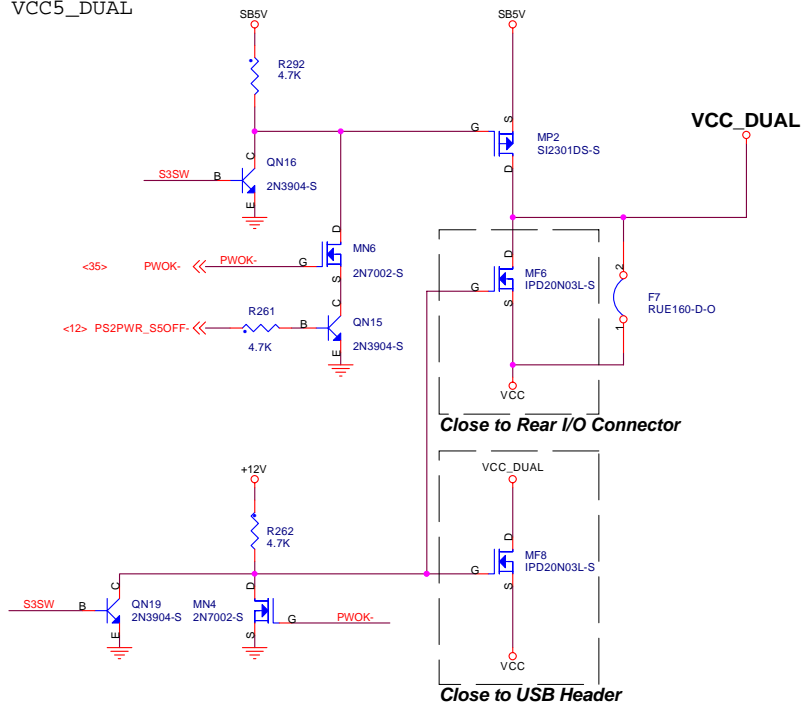
AUTO VOLTAGE SWITCH FOR ACPI STATE 3

1.IN S0,S1
THIS CIRCUIT PASSES THE NORMAL POWER

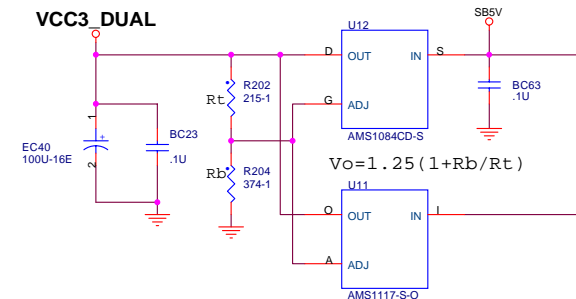
2.IN S3,S4,S5
THIS CIRCUIT PASSES THE STANDBY POWER

NOTE:
BECAUSE OF THE MAXIMUM CURRENT FROM
POWER SUPPLY IS ONLY ABOUT 750-1000mA
SO IF YOU WANT TO SUPPORT WAKE UP
FROM S3 BY USB, YOU MUST HAVE A POWER
SUPPLY WITH LARGER POWER. (ADDITIONAL
500mA PER USB PORT)

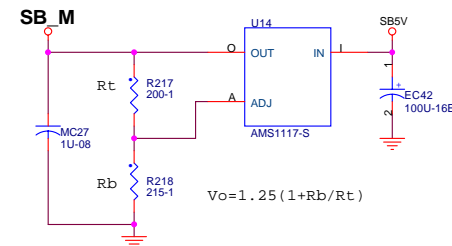
VCC3_DUAL & VCC5_DUAL



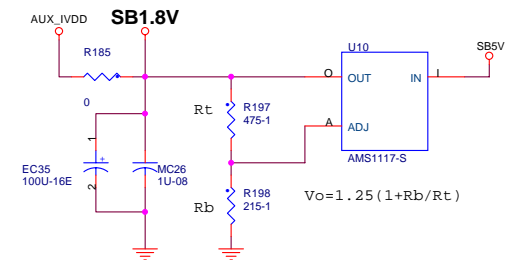
VCC3_DUAL



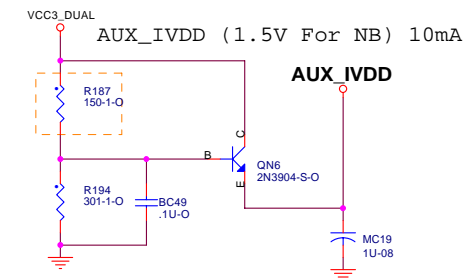
SB_M



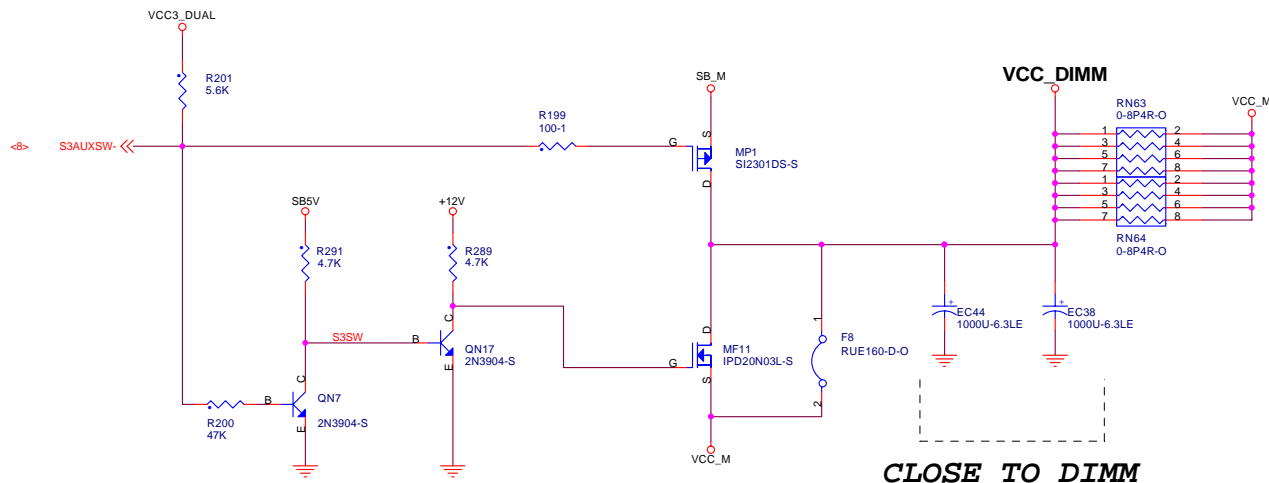
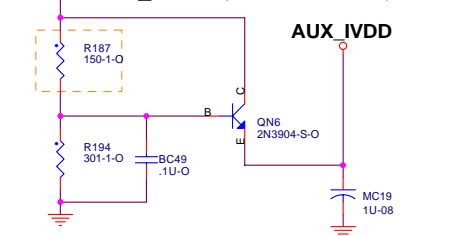
SB1.8V (For SB) 450mA



VCC3_DUAL



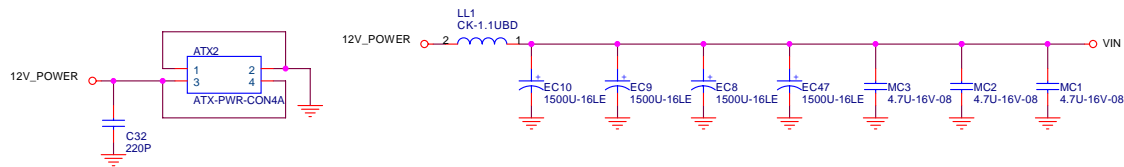
AUX_IVDD (1.5V For NB) 10mA



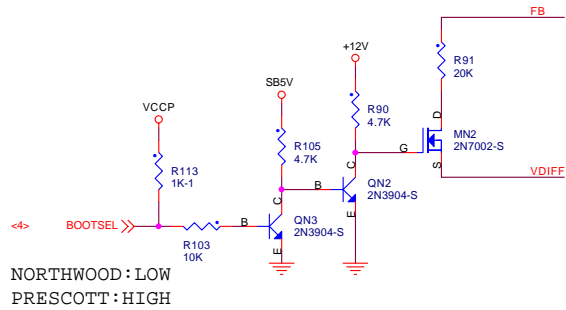
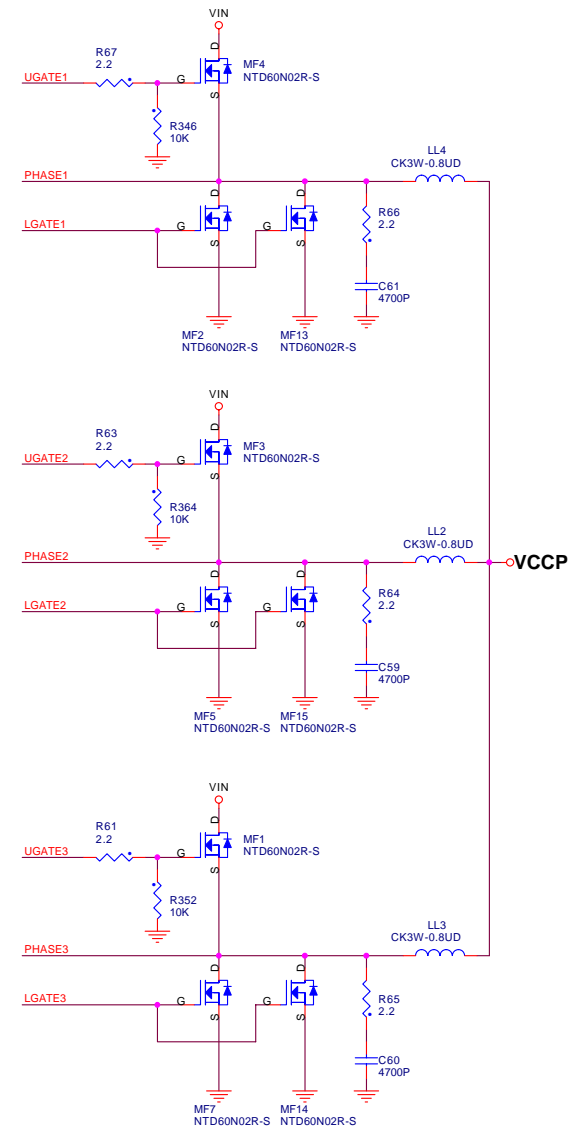
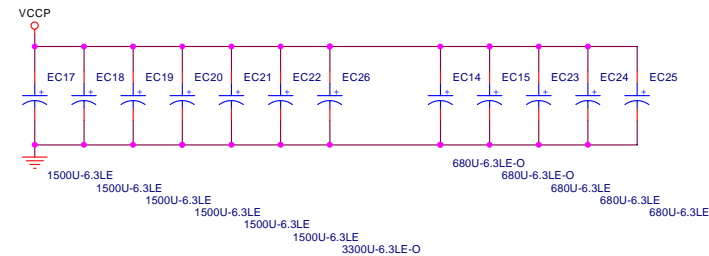
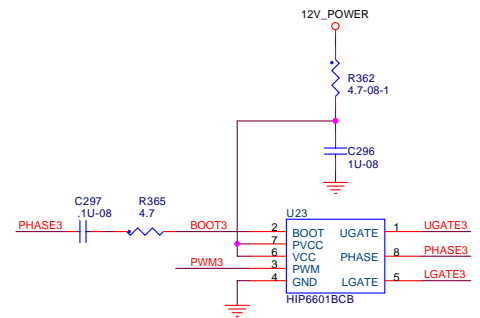
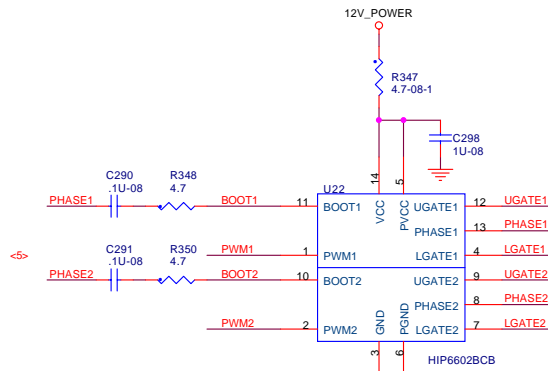
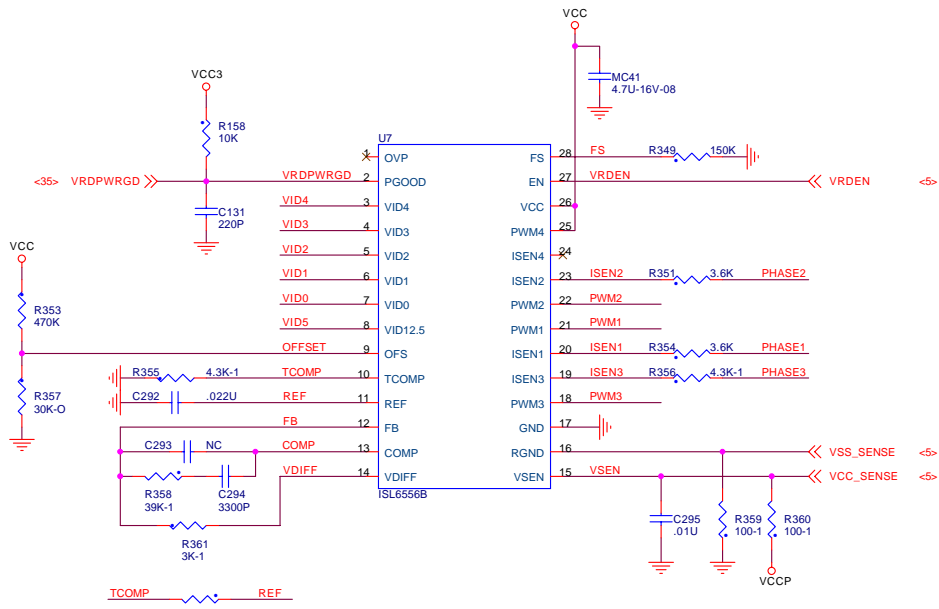
CLOSE TO DIMM

litegroup Computer Systems

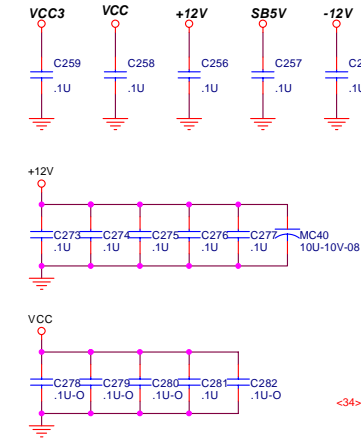
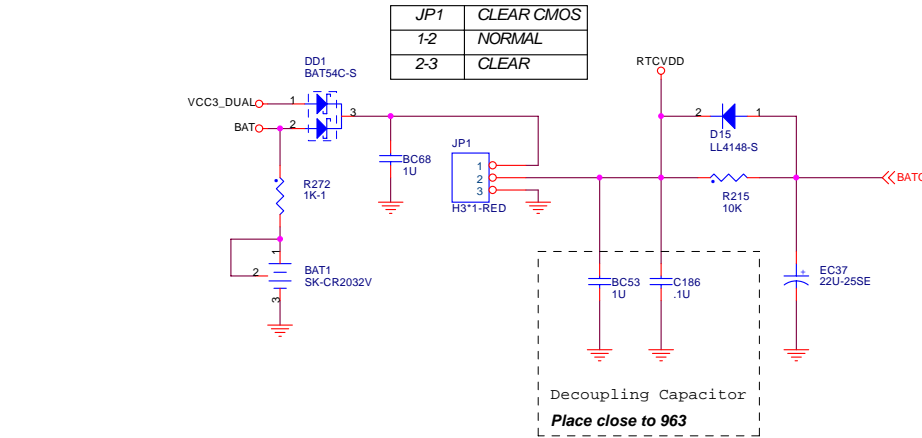
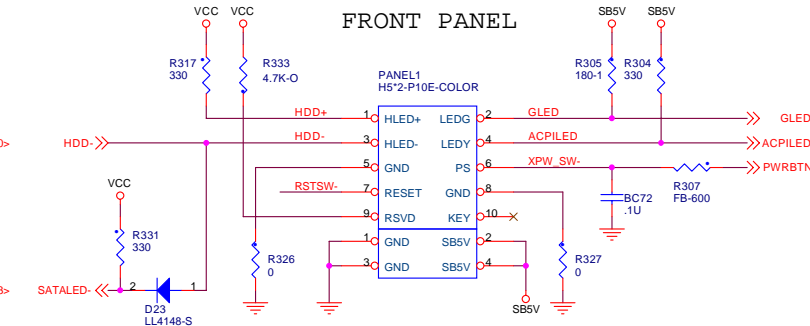
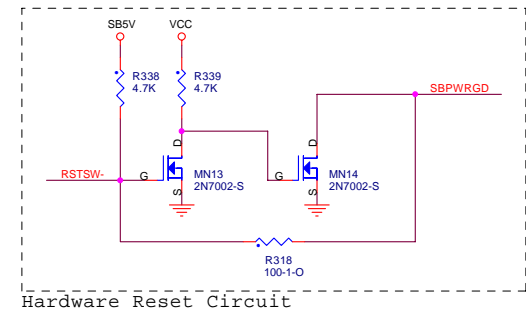
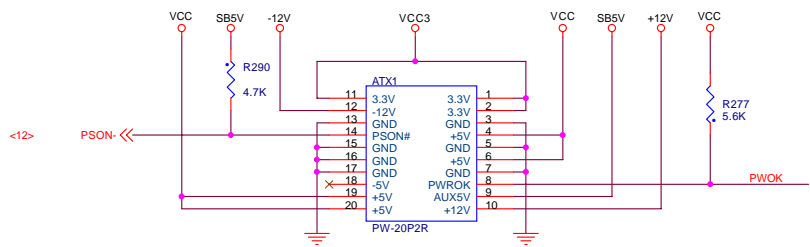
Title			SF2 / 661FX	
Size	Document Number	Dual 5V&3V, STR		Rev
Custom				2.2
Date:	Monday, December 29, 2003	Sheet	33 of 36	



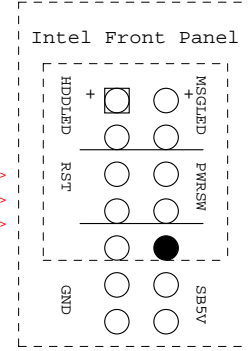
<4> VID[0.5] >> VID[0.5]



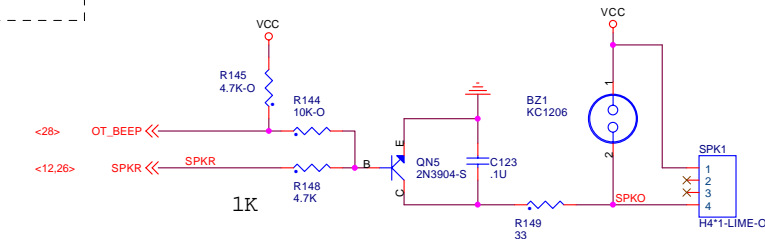
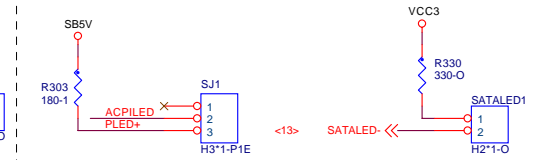
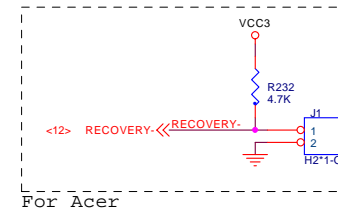
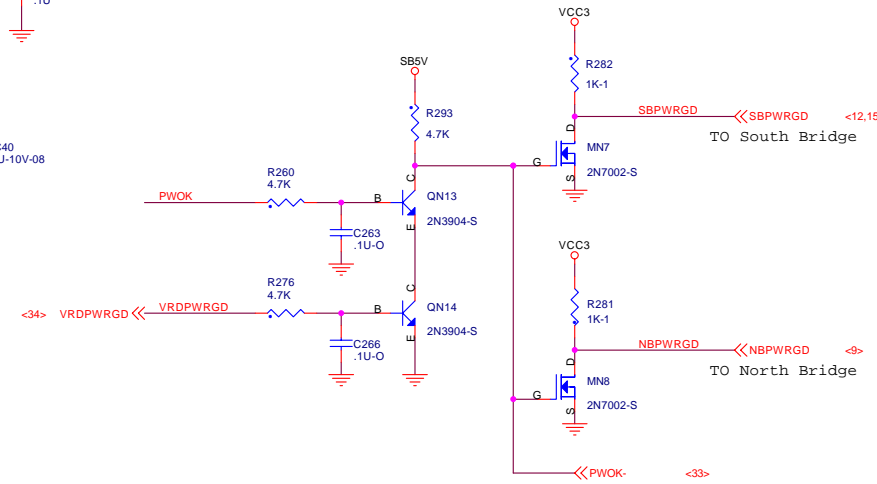
NORTHWOOD: LOW
PRESCOTT: HIGH



Acer Front Panel



Layout :
Bypass capacitors close to ATX power connector for EMI solution.



NOTE!
1.The RTCVDD is 3V
2.Decoupling capacitor must be close to 635 RTCVDD pin.
3.RTC circuit must strictly follow SiS's recommended design
SiS is not responsible for RTC problems from foreign designs.

1. BOM Attention

(1) SATA

Option Components	Yes	No
U13	964	964L
R241	374	X
R71, R74	33	X
R72, R75	49.9	X
R331	330	X
D23	1N4148	X
SATA1, SATA2	O	X

(2) LAN

Option Components	10/100 Mbps	1Gbps
LAN1	RTL8100C	RTL8110S
R53	5.6K	2.49K
R12, R14, R21, R28	X	49.9
C10, C18	X	0.1u
C51	0.1u	0.01u
C52, C53, C54	X	0.01u
RN62	75-8P4R	X
R62	X	0 ohm
T1	LF-H59X	HQ-H40B
L14	X	0 ohm
C23	X	0.1u
L21	0 ohm	X
QP1	X	HA8550
R321	0 ohm	X
R322	X	0 ohm
L10	0 ohm	X

(3) On-Board VGA

Option Components	Support	No Support
U8	661FX	648FX
L30, L31, L32	FB-120	X
C112, C116, C117, BC35	1U	X
C118, C119	.1U	X
MC36, MC37	10U	X
R136	130	X
R134, R143	33	X
R128, R135	100	X
VGA1	O	X
L6, L7, L8	FB-80	X
C111, C114, C115	22P	X
R22, R23, R24	75	X
R32, R39	2.2K	X
CV1~7	22P	X
F2	O	X
R234	475	169
R248	1K	301
R197	475	374
R198	215	200

2. GPIO Function

GPIO	Status	0	1	Jumper
GPIO5	* Clear CMOS for HP	Clear CMOS	Normal	JP4
GPIO6	* Clear Password for HP	Clear Password	Normal	JP5
GPIO7	* RESERVED	RESERVED	RESERVED	N/A
GPIO9	USB, PS/2 S4/S5 Wake Up	Disable	Enable	N/A
GPIO10	DDR Voltage	2.54V	2.63V	N/A
GPIO11	* WHQL	No Support	Support	JPT3

(1) "*" means that the function is selective and ECS may make changes at any time, without notice in this page.

(2) Jumper Setting (Header 3*1):

1: (1-2)

0: (2-3)

(3) Please see Page.12 for more detail jumper function.

